Samsung Research

RISC-V: The Open Accelerator Platform for Modern Workloads

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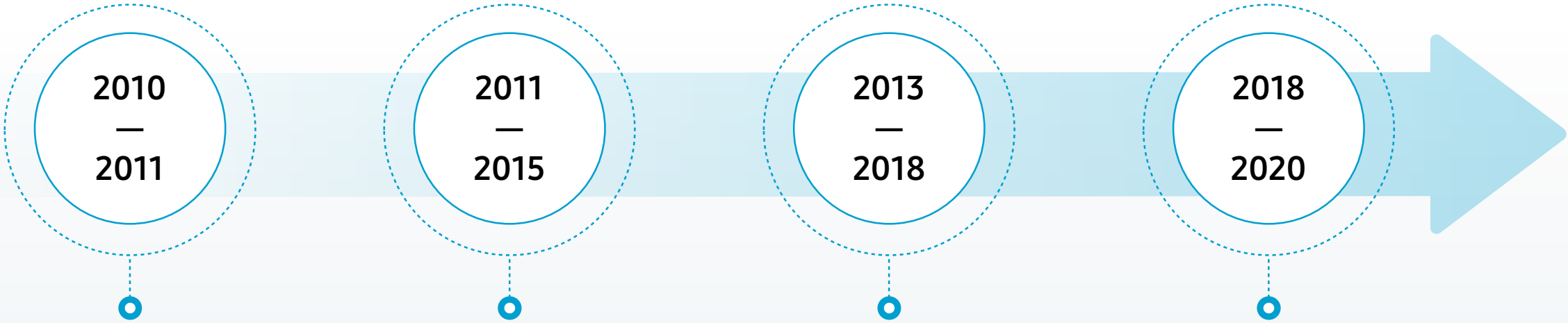
Brief history



Inception

UC Berkeley's Par Lab (Prof. Krste Asanović, Yunsup Lee, and Andrew Waterman), with the first RISC-V Instruction Set Manual published in May 2011.

RISC-V Foundation

The first RISC-V chip tape-out (2011), a foundational paper advocating open instruction sets (2014), and the launch of the RISC-V Foundation (2015).

DARPA Influence

The ASPIRE Lab received DARPA and corporate funding. RISC-V systems were used to support power-efficient embedded computing research under DARPA's PERFECT program.

RISC-V International

In response to geopolitical concerns, the RISC-V Foundation collaborated with the Linux Foundation (2018) and moved its incorporation to Switzerland, forming RISC-V International in 2020.

Open ISA with Extensions

Since its inception, RISC-V has been a **royalty-free, open ISA** (Instruction Set Architecture). Unlike proprietary ISAs (such as ARM or x86), RISC-V enables anyone to **design, implement, and modify** processors based on its specifications.

The RISC-V ISA is designed with **modularity and extensibility** in mind:
base integer ISA (RV32I/RV64I/RV32E/...) with optional extensions (e.g., MAFDC).
As for November 2024, there are about **130 ratified extensions**.

RISC-V non-ISA specifications: trace, debug, ABI, interrupts, IOMMU, firmware, etc.

RISC-V Profiles: RVA23/RVB23 (October 2024), specifying mandatory, optional, development, and expansion extensions.

> The primary goal of the RVA profiles is to align processor vendors targeting binary software markets, so software can rely on the existence of a certain set of ISA features in a particular generation of RISC-V implementations.

RVV Basics

- First proposal presented in June 2015, **ratified in November 2021**, with additional extensions ratified in 2023 (half-precision, crypto).
- **SIMD extension**, similar to SSE, AVX, Neon, SVE, but different.
- **Over 180 instructions** (largest to date) with highly configurable load/store operations: unit-stride, constant-stride, indexed (gather-scatter), segment.
- **VLEN (Vector Register Length)** – an implementation parameter – dynamic vector length at runtime.
- **Data types (SEW):** 8/16/32/64-bit signed/unsigned integers, 16/32/64-bit floats.
- **Additional features:** register grouping (LMUL), element masking, tail/mask agnostic policies.

Valuable materials:

- ARM vs RISC-V Vector Extensions – Erik Engheim
- RISC-V Vector Extension overview – Wojciech Muła
- Next-Generation Vector Processor Design webinar series – Andes Technology

Hardware Availability (RVV1.0)

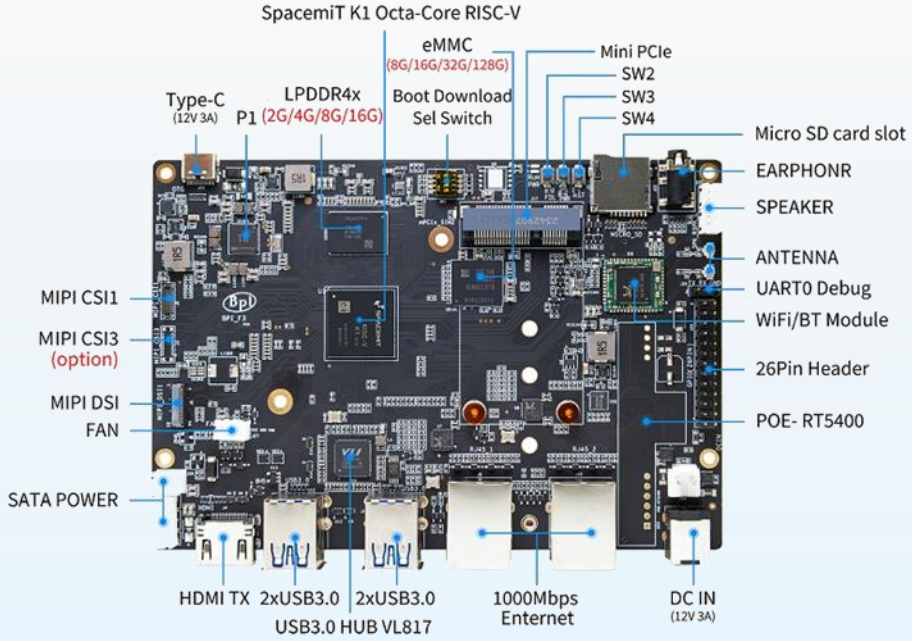
RVV-capable open-source IP

- “Small” vectors (Zve64d, Snitch + Spatz)
  Spatz: Clustering Compact RISC-V-Based Vector Units to Maximize Computing Efficiency
- “Medium” vectors (Shuttle + Saturn) with Linux support
  The Saturn Vector Unit: Design of a Fully Compliant Open-Source RISC-V Vector Unit
- “Big” vectors (CVA6 + PULP Ara) with Linux support
  Ara2: Exploring Single- and Multi-Core Vector Processing with an Efficient RVV 1.0 Compliant Open-Source Processor

There are also closed solutions from commercial vendors.

Available boards

- CanMV-K230 (Canaan K230, single-core, VLEN=128).
- BananaPi-F3 and DC-ROMA Laptop II (SpacemiT K1, octa-core, VLEN=256) – the first SoC viable for development on hardware.



Software availability

- Official or semi-official support for RISC-V in Ubuntu, Debian, Fedora.
- Reliable development under QEMU with GDB stub support, and option to set VLEN.
- Intensive upstream work in open source system libraries by community and companies.
- Extension auto-detection in Linux from version 6.4.

GNU toolchain

- ✓ Full support for RVV1.0 (and RVA23).
- ✓ Autovectorization supported since version 14.
- ✓ Debugger (GDB) is somewhat working but still lacking some important features.

GCC 14 RISC-V Vectorization Improvements and Future Work – Robin Dapp, Ventana

LLVM toolchain

- ✓ Full support for RVV1.0 (and RVA23).
- ✓ Autovectorization supported since version 19.
- ✓ Debugger (LLDB) – basic RISC-V support is landing in version 20.

RISC-V LLVM State of the Union – Alex Bradbury, Igalia

Case Study: What do we do at Samsung?

RISE

Premier member of RISE (RISC-V Software Ecosystem Project) – working on system libraries, toolchains, language support, and others.

RVV

- Experiments with **virtual RVV-capable targets**
  Accelerating Software Development for Emerging ISA Extensions with Cloud-Based FPGAs
- Adding **RVV support** to system libraries:
  Pixman, GStreamer Orc, Opus.
- **Extending CI** support for multi-platform library testing
  CI Setup for Multi-Platform Software Projects

Tizen OS

Board bring-up and support for Tizen OS, including support for product divisions.

Case Studies

cea list

European Processor Initiative

epi

TRISTAN

VRP: a Variable extended Precision Accelerator for Scientific Computing Applications

Andrea Bocco, A. Hoffmann, E. Guthmuller, C Fuguet, Y. Durand, J. Fereyre, I. Tahir, R. Alidori, T. Khandelwal, N. Perbost

RISC-V summit Munich 24-28 Juin 2024

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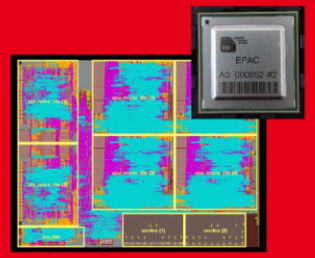


RISC-V SUMMIT EU

JUNE 24 - 28 | MUNICH 2024

26/06/2024

Barcelona Supercomputing Center

Centro Nacional de Supercomputación

RISC-V@BSC: Fostering RISC-V strategy in Europe through Research, Innovation & Education

PhD. Teresa Cervero

RISC-V Summit Europe 2024

ETH zürich · ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA

Towards Neuromorphic Acceleration through Register-Streaming Extensions on RISC-V Cores

University of Bologna

Simone Manoni s.manoni@unibo.it
Paul Scheffler
Alfio Di Mauro
Luca Zanatta
Andrea Acquaviva
Luca Benini
Andrea Bartolini

PULP Platform
Open Source Hardware, the way it should be!

@pulp_platform
pulp-platform.org
youtube.com/pulp_platform

AXELERA ARTIFICIAL INTELLIGENCE

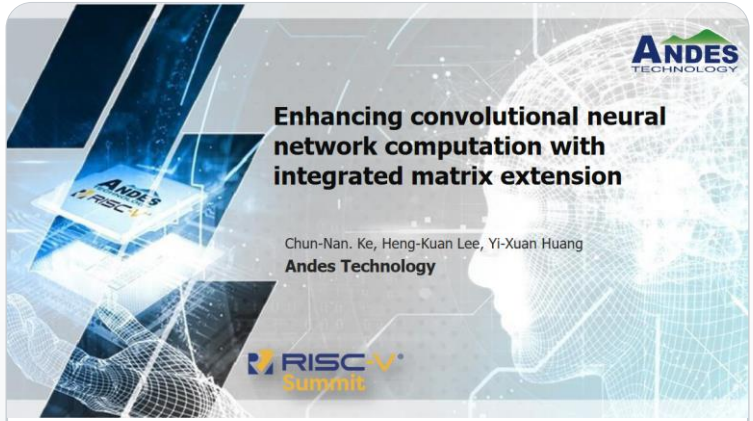
Simplifying AI at the Edge.
Accelerating Computer Vision.

Accelerating Edge AI with RISC-V

Florian Zaruba

November 7th, 2023

On the Horizon



Matrix Extensions

IME – built on top of RVV.
AME – tightly coupled but self-contained.

AI/ML Accelerators

Outlook onto the future ways of customizing AI/ML acceleration.

Scale of adoption

Estimated 30% market share of shipped SoCs by 2030 in key markets.

Core-V eXtension Interface (CV-X-IF)

Standardized interface for extending the CPU with custom instructions. Already implemented in CV32E40X and CVA6 with more to come.

4. Summary

Freedom to customize the feature set – scalable from embedded/edge applications to high performance AI/HPC workloads.

RISC-V offers a thriving ecosystem with robust software development tools, and production-ready IP.

Backed by an active global community of commercial and academic partners, ensuring strategic stability.

Samsung Research

Thank you!

Questions?

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