

TU Delft – Accelerated BigData Systems

# Enhanced Development with Typed Hardware

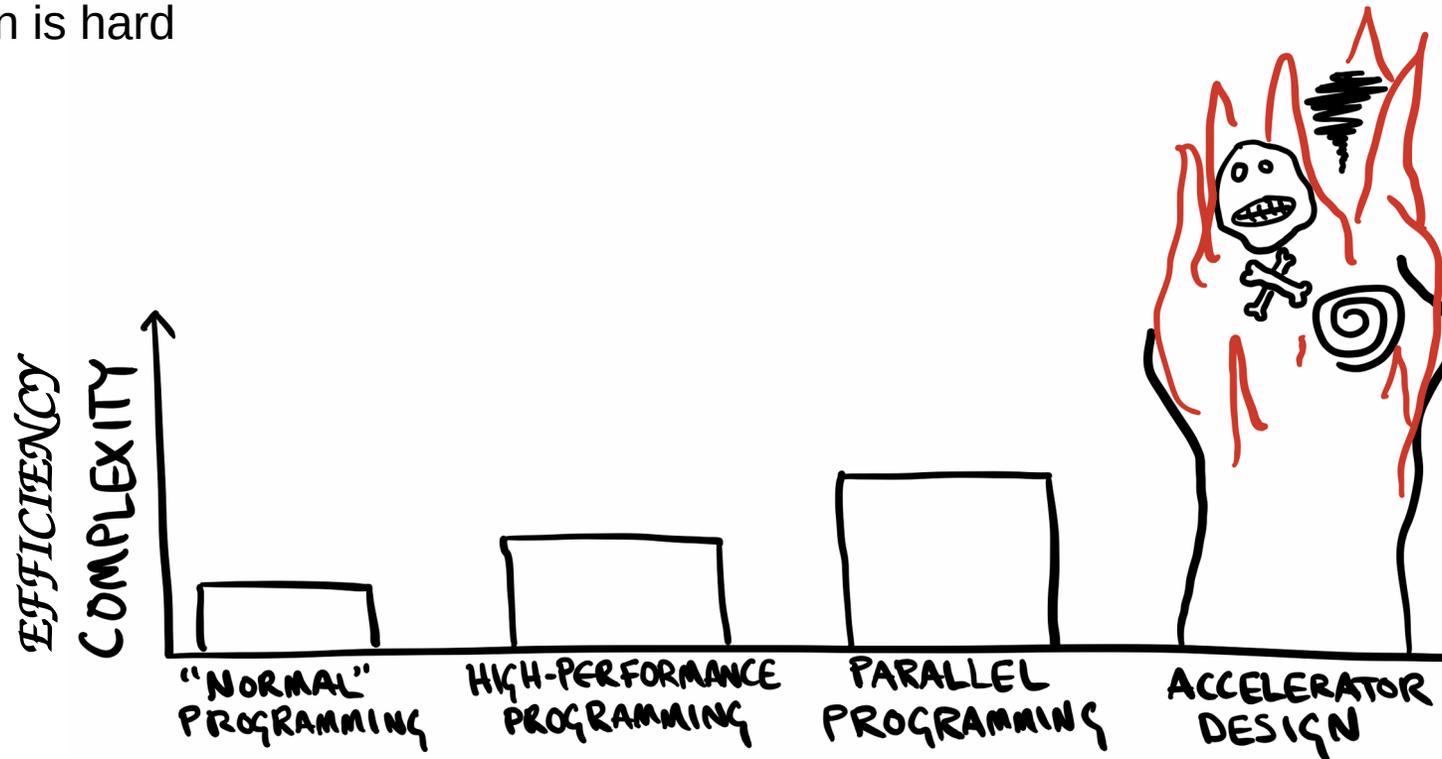
Casper Cromjongh

06-12-2024

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# The Problem

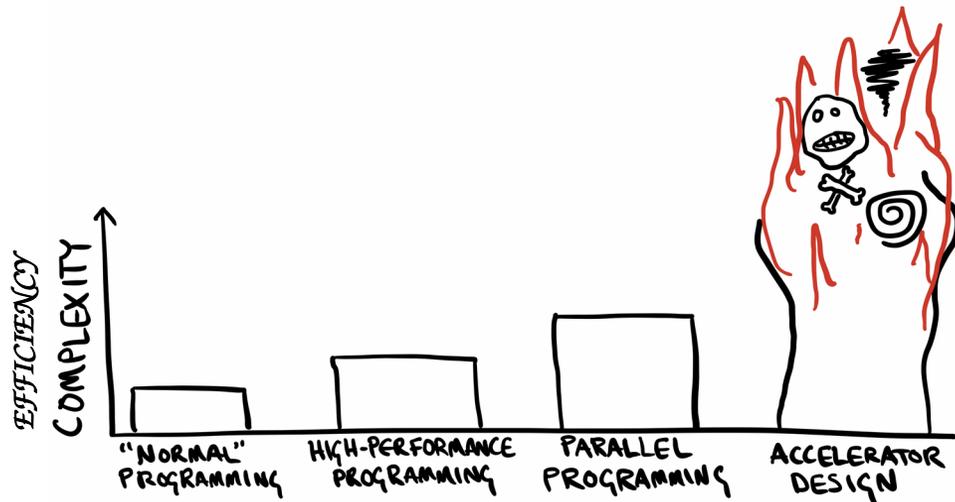
- Hardware design is hard



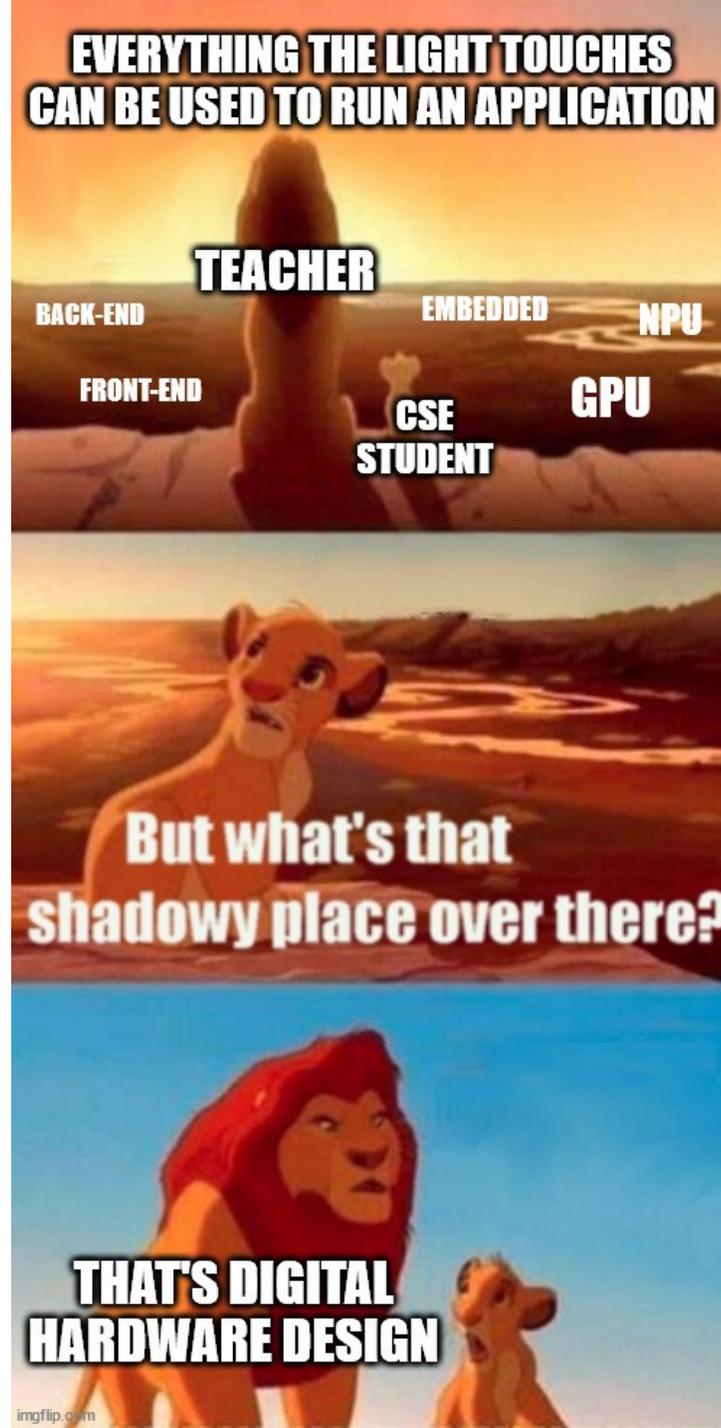
<https://www.sigarch.org/hdl-to-ad/>

# The Problem

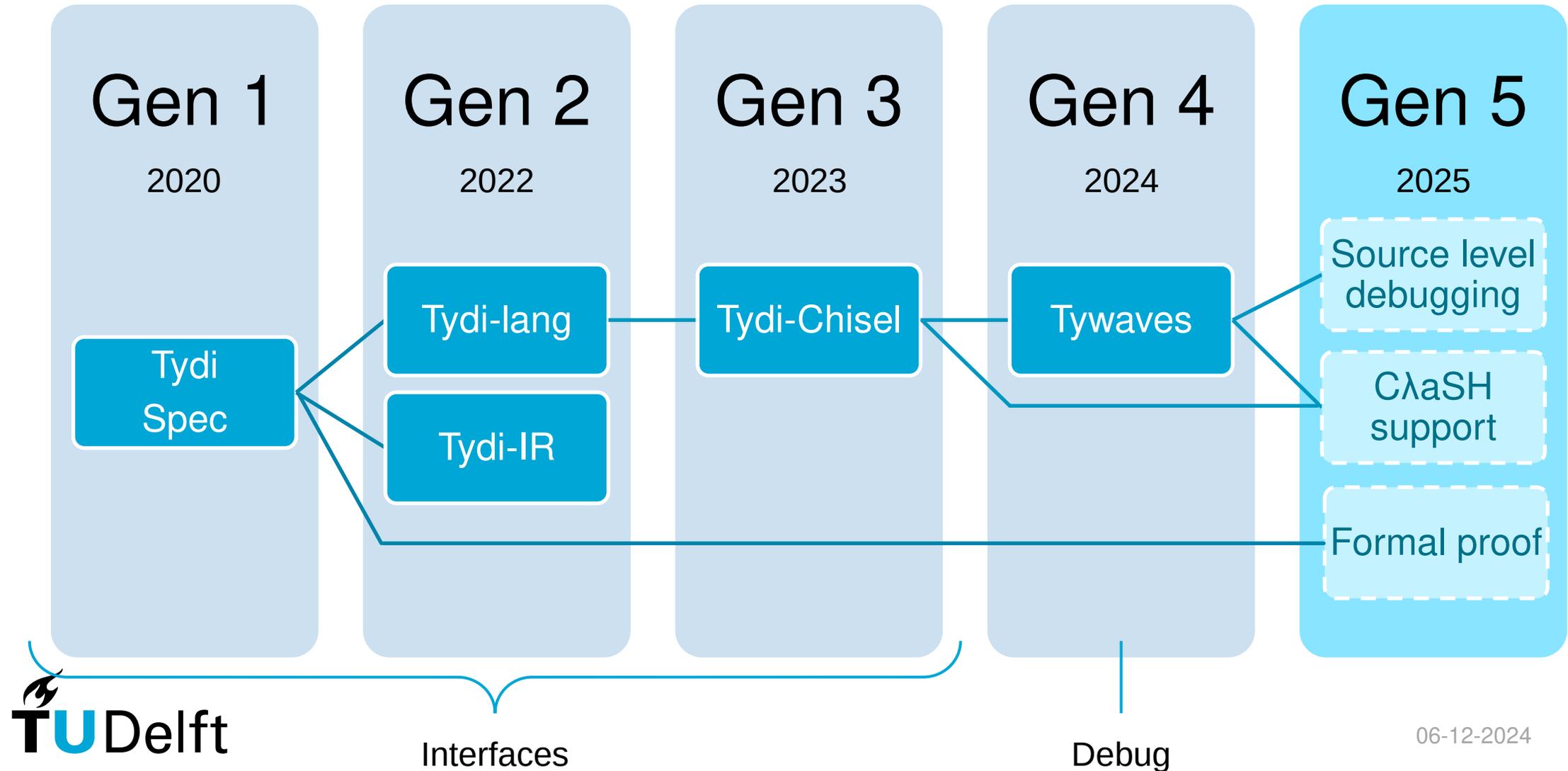
- Hardware design is hard
- Software is easy to use
- Why is hardware not?



<https://www.sigarch.org/hdl-to-ad/>



# Typed Hardware Research @ ABS TU Delft



# Typed Hardware Research @ ABS TU Delft

Tydi-Chisel

**Tydi implementation in Chisel & PoC systems**

Presented here last year

Tywaves

**Typed waveform viewer for Chisel, conserving high level types**

By Raffaella Meloni

Source level  
debugging

**Improve typed debugging with breakpoints and source navigation**

By Jarl Brand

Clash  
support

**Tydi protocol implementation in clash-protocols**

By Marijn Adriaanse in collab. with 

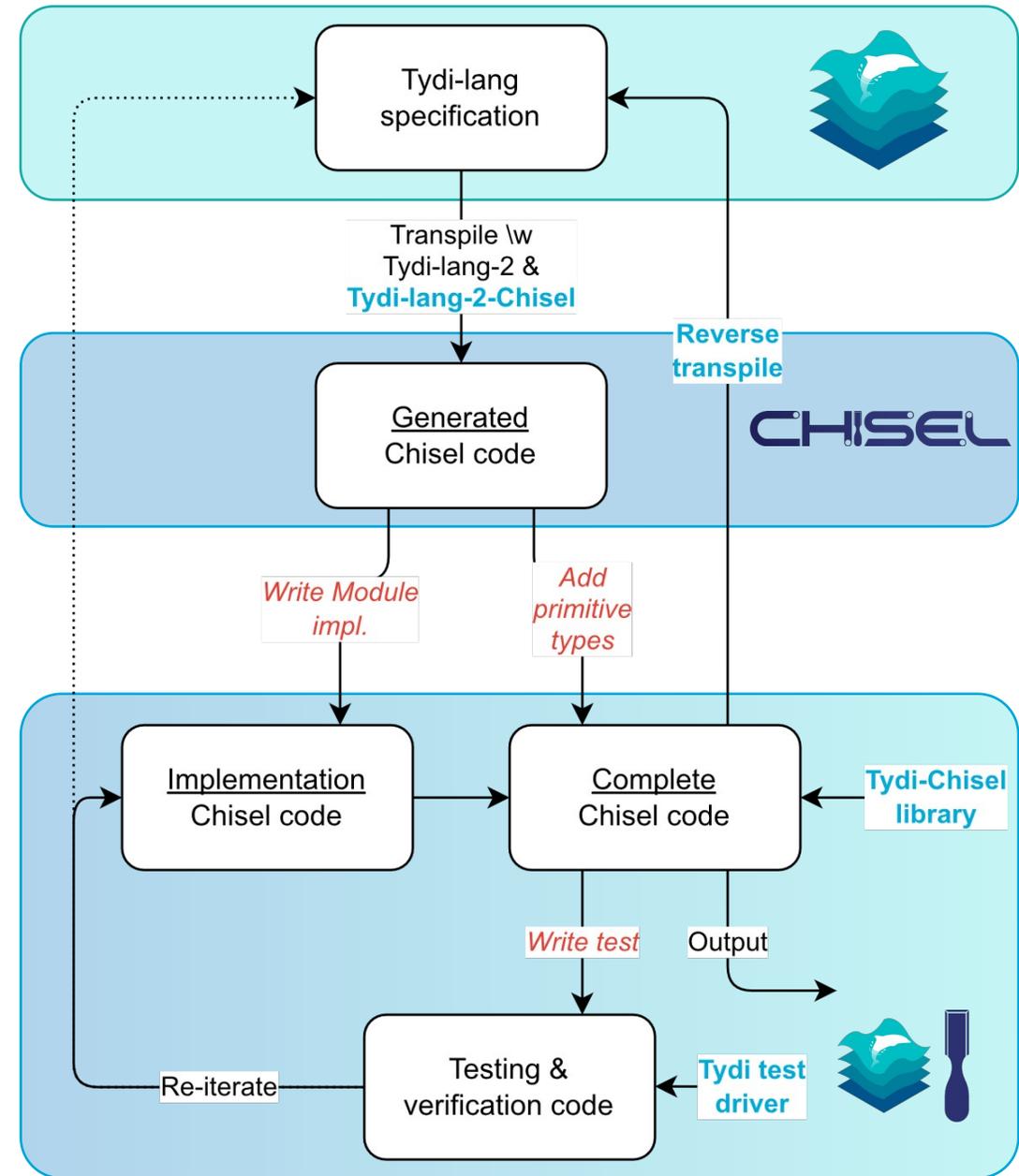
Formal proof

**Verify Tydi-Spec type system principles and timing guarantees**

By Harold Struik

# Tydi-Chisel

- Component *interface standard*
- *Software like abstractions* for *data types* in hardware
- Support any data-hierarchy
  - Support nested lists
- Integrate in existing tooling



# Tywaves

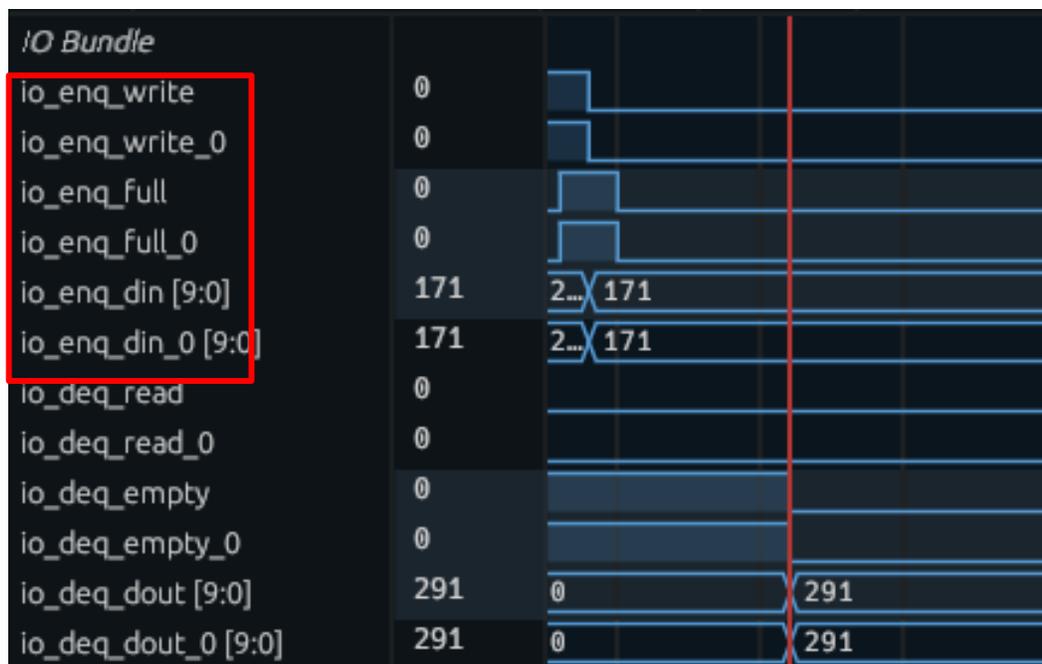
- Typed **waveform viewer** for Chisel
- Conserve *high level types* through *Verilog simulation*

- *Solves:*

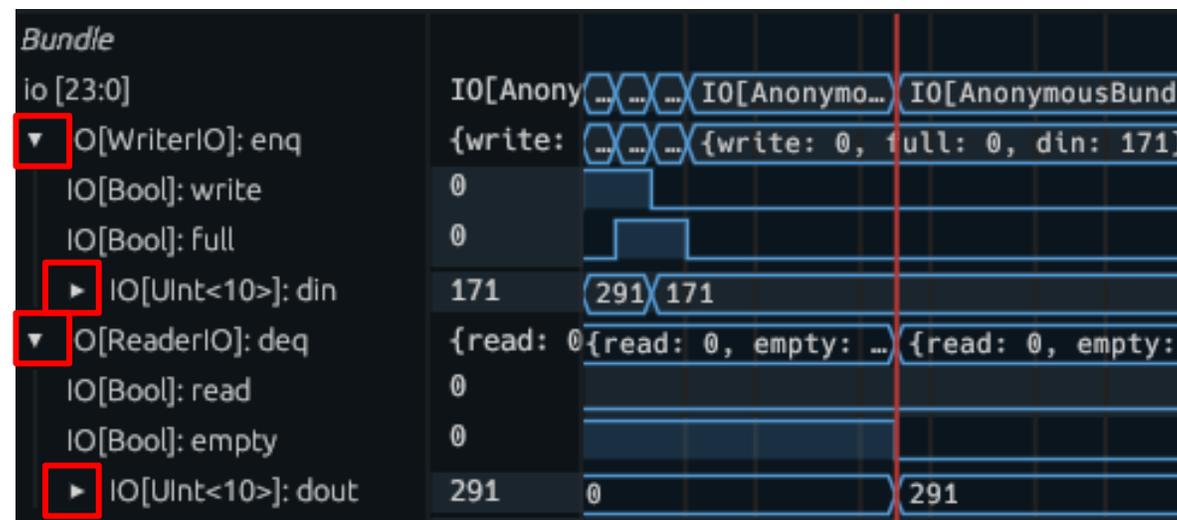
What the user writes  What the user sees

# Tywaves

Only VCD

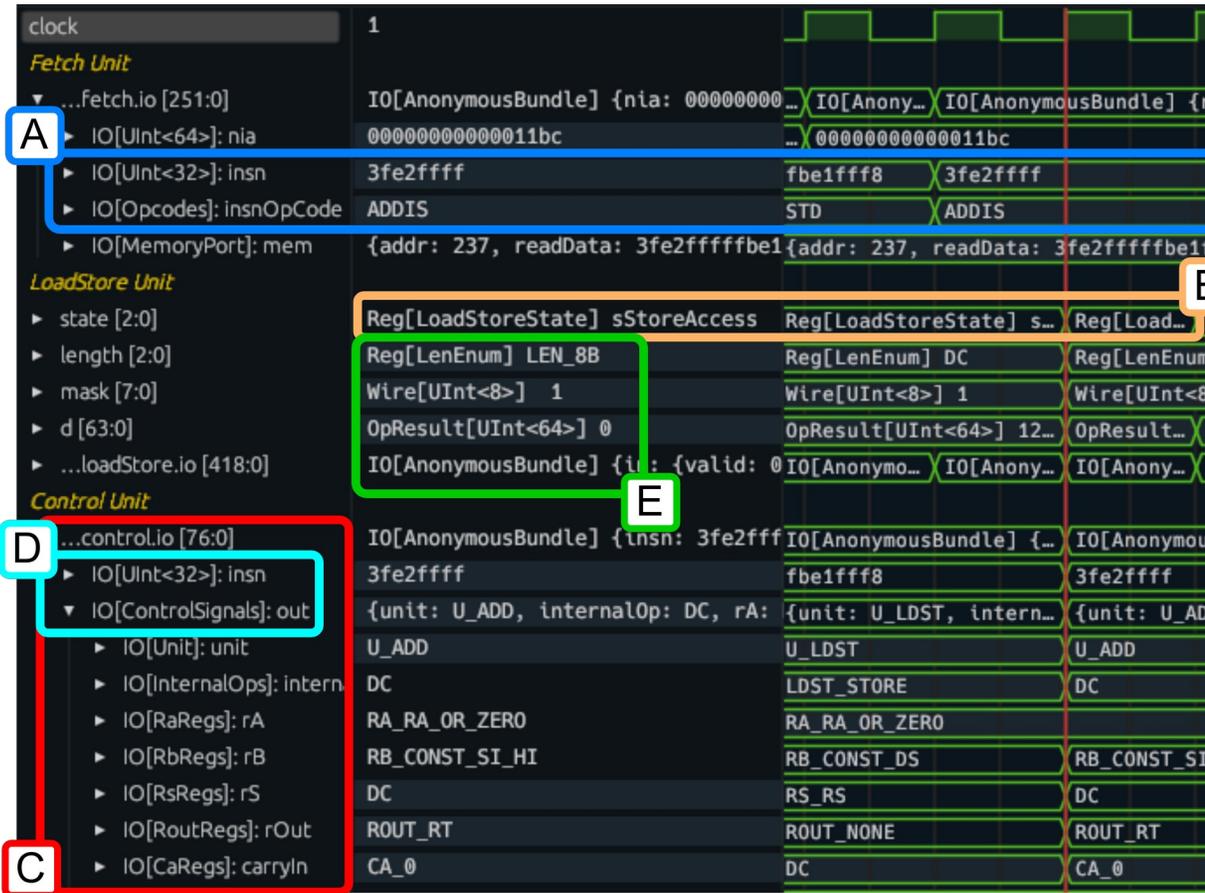


Tywaves enabled

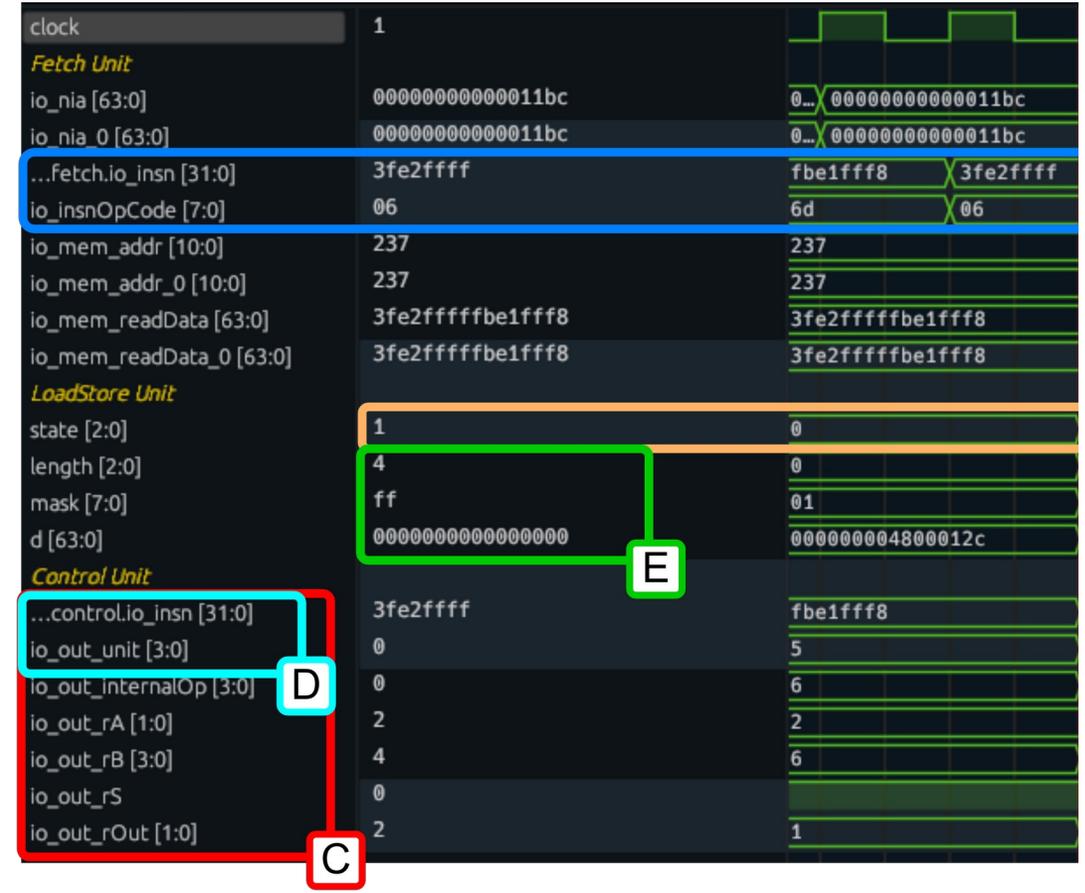


# Tywaves – Chiselwatt simulation

Tywaves display



VCD only display



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# Typed Hardware development



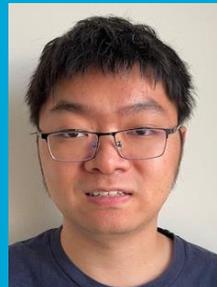
Casper  
Cromjongh



Zaid  
Al-Ars



Christiaan  
Boerkamp



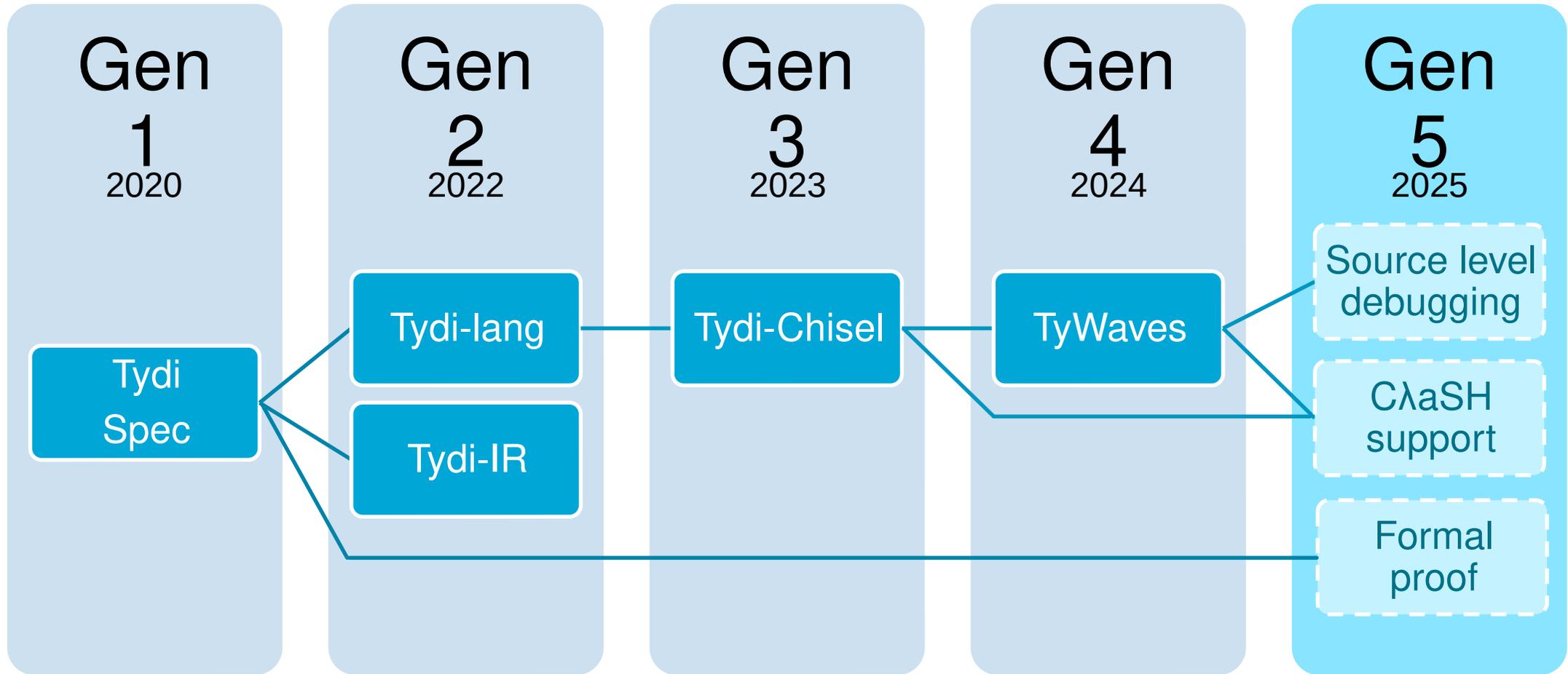
Yongding  
Tian

(and others  
from ABS)

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[github.com/abs-tudelft](https://github.com/abs-tudelft)

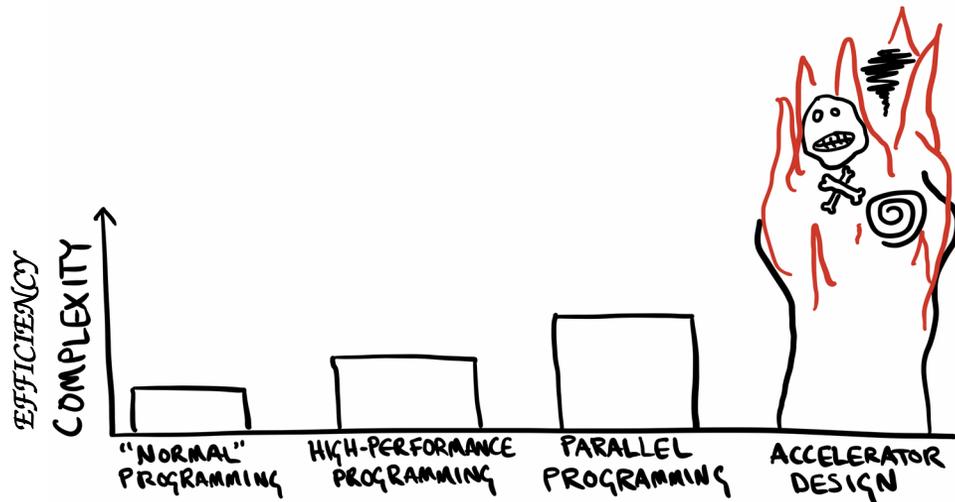
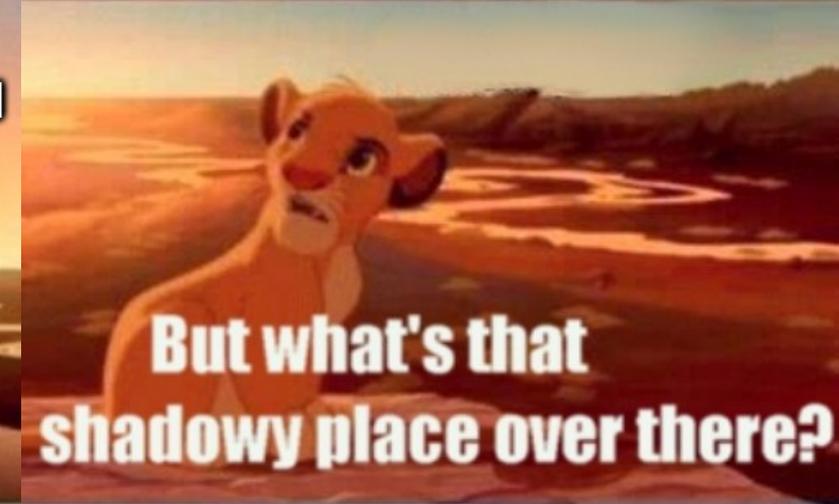
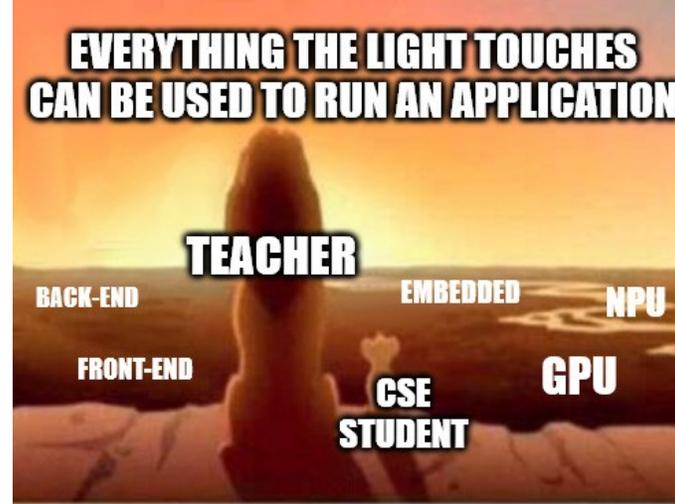
Thank you for your attention

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