Master Project Proposals
(Related to Cryogenic Electronics)

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TU Delft

10 Steps of M.Sc. Projects

1- Understanding the requirements of the targeted application/system

2- Defining the specification of your block

3- Literature review on cryo-CMOS circuits and on the architectures of your specific block

4- Performing system analysis and finding the optimum structure

5- Simulating the circuit in cadence→ Finding the related issues→ Finding novel solutions

6- Circuit design in 40-nm CMOS or 22-nm FinFET technology

7- Layout of test chip and Post layout simulations

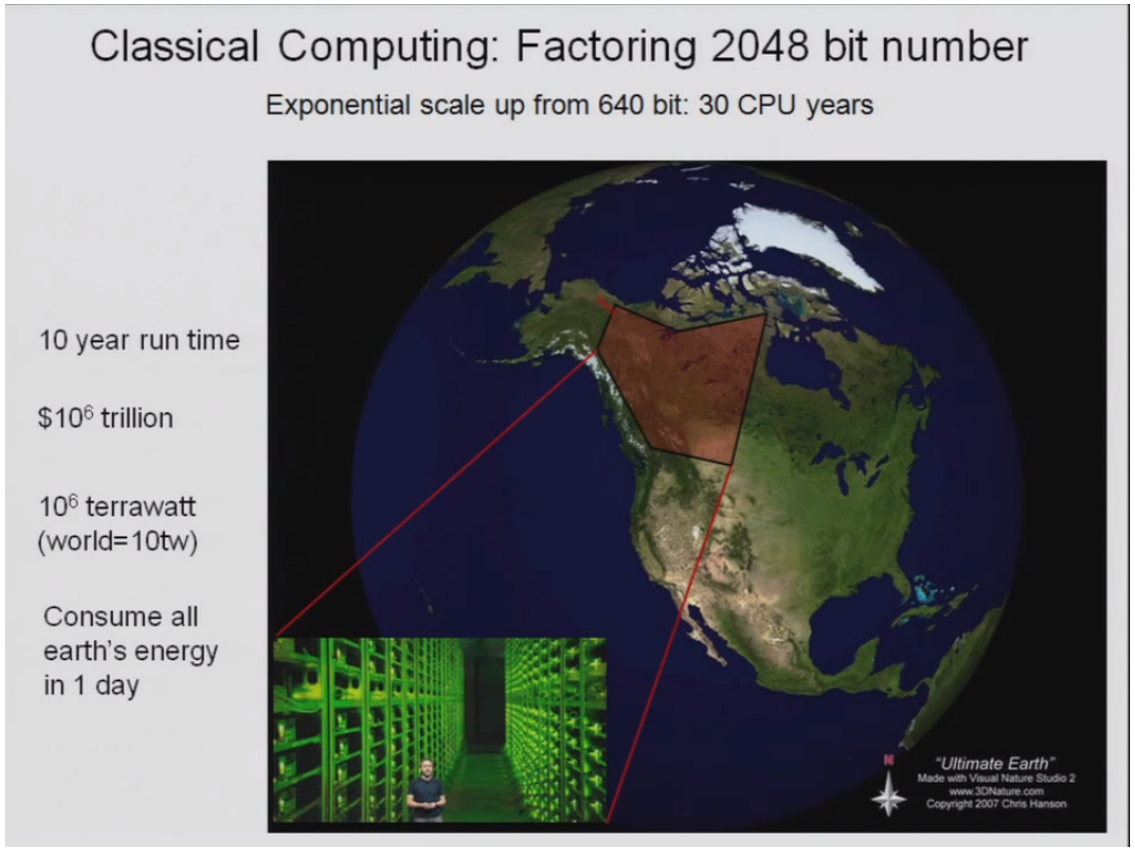
8- Preparing measurement setup

9- Measurement and analysing the measured performance of the chip

10- Writing the thesis, paper, …

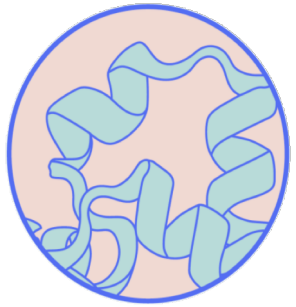
Cryogenic RF Blocks for Control and Readout of Quantum Bits

Need for Quantum Computers

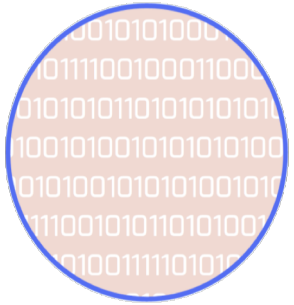


Encryption/decryption

Protein folding

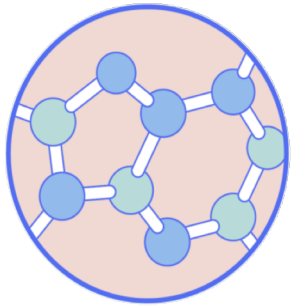


Big data



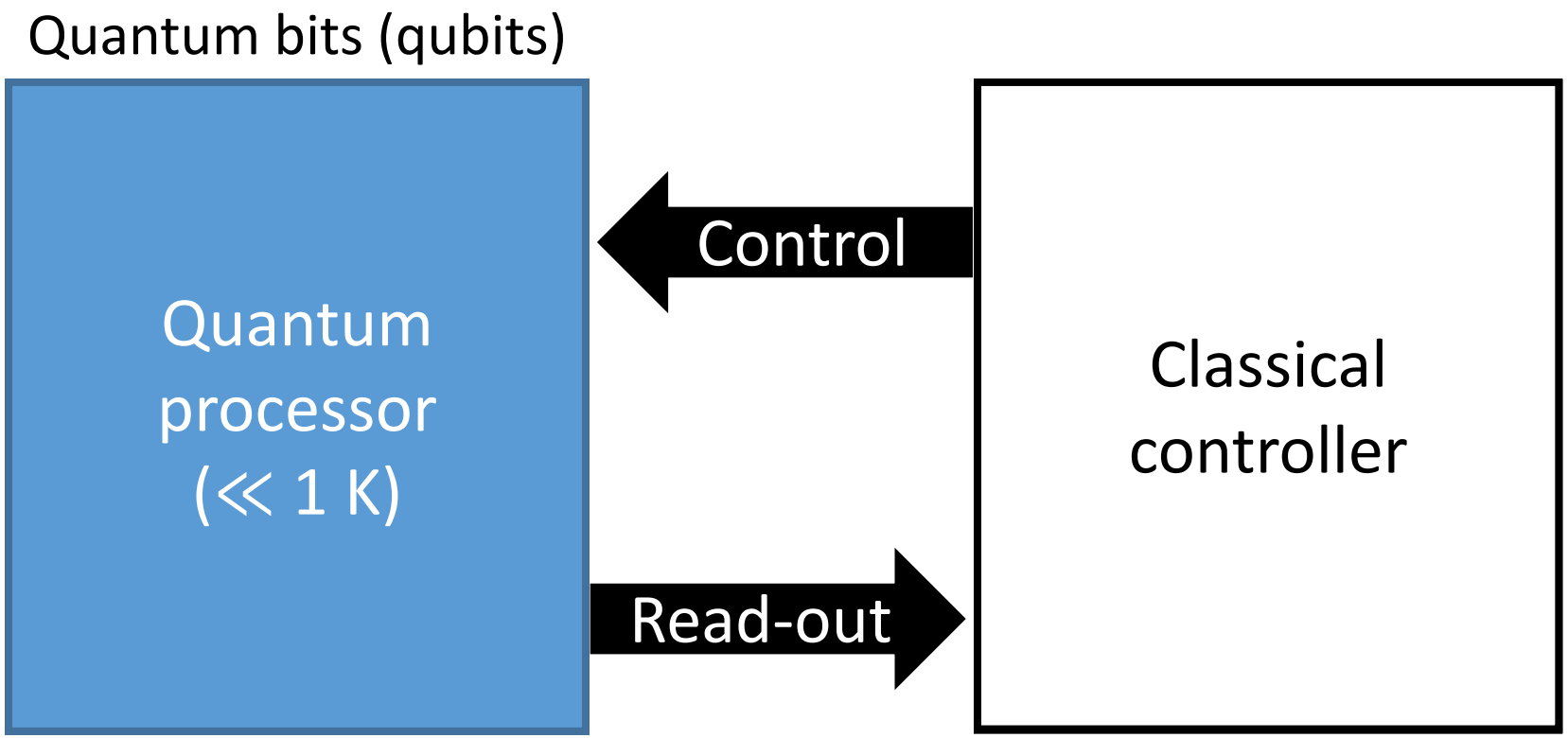
Drug synthesis

Molecule simulation



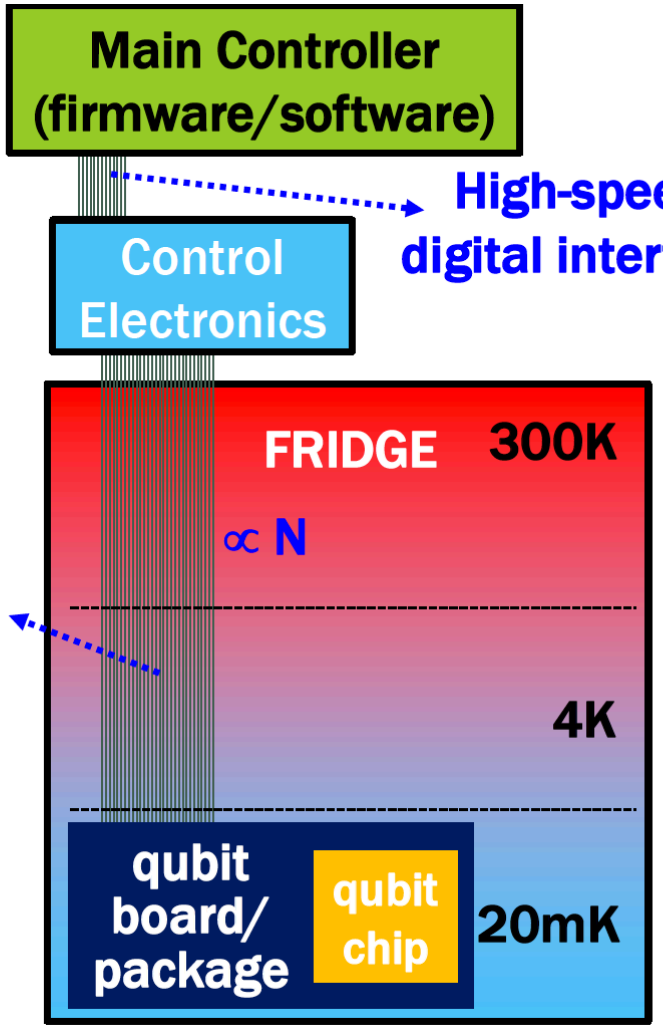
DNA analysis

Quantum Computer Architecture

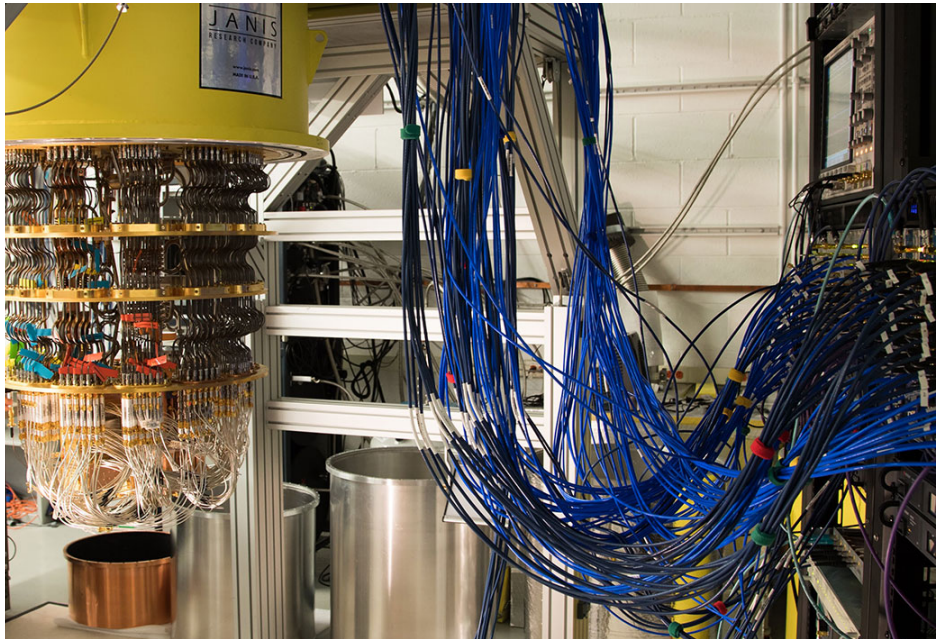


- Carrier frequency: 100 MHz – 20 GHz
- Pulses: 10 – 500 ns

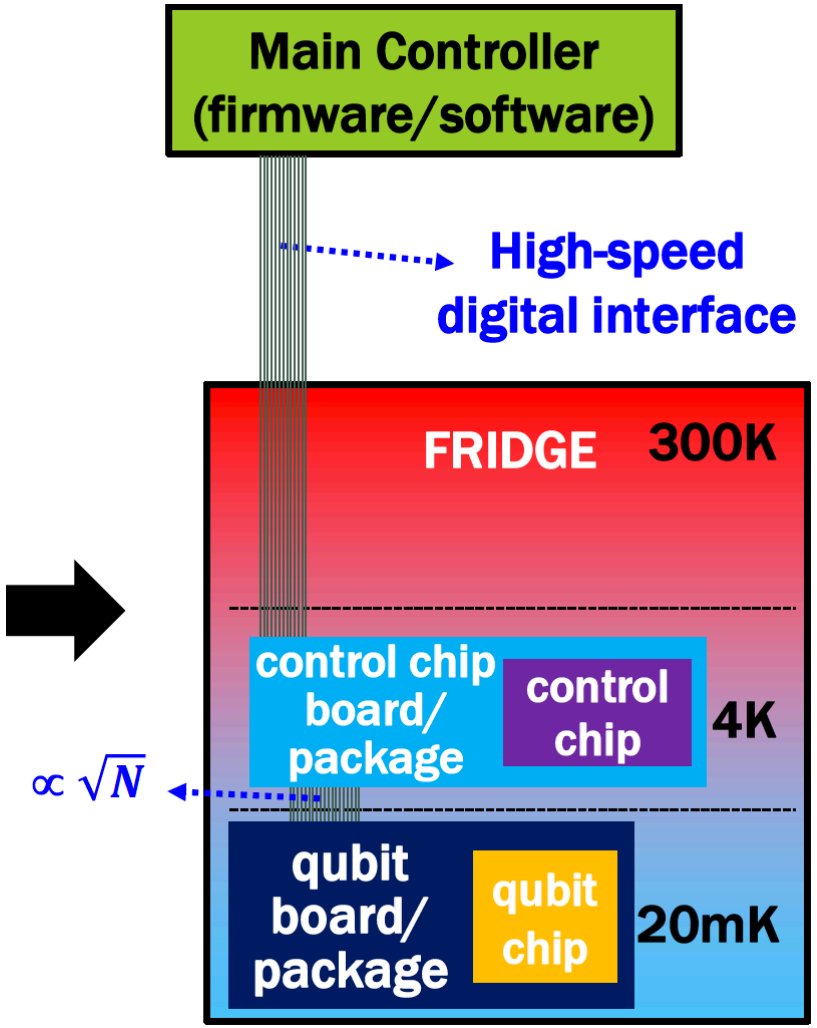
Need for Highly Integrated Cryogenic Qubit Control and Readout



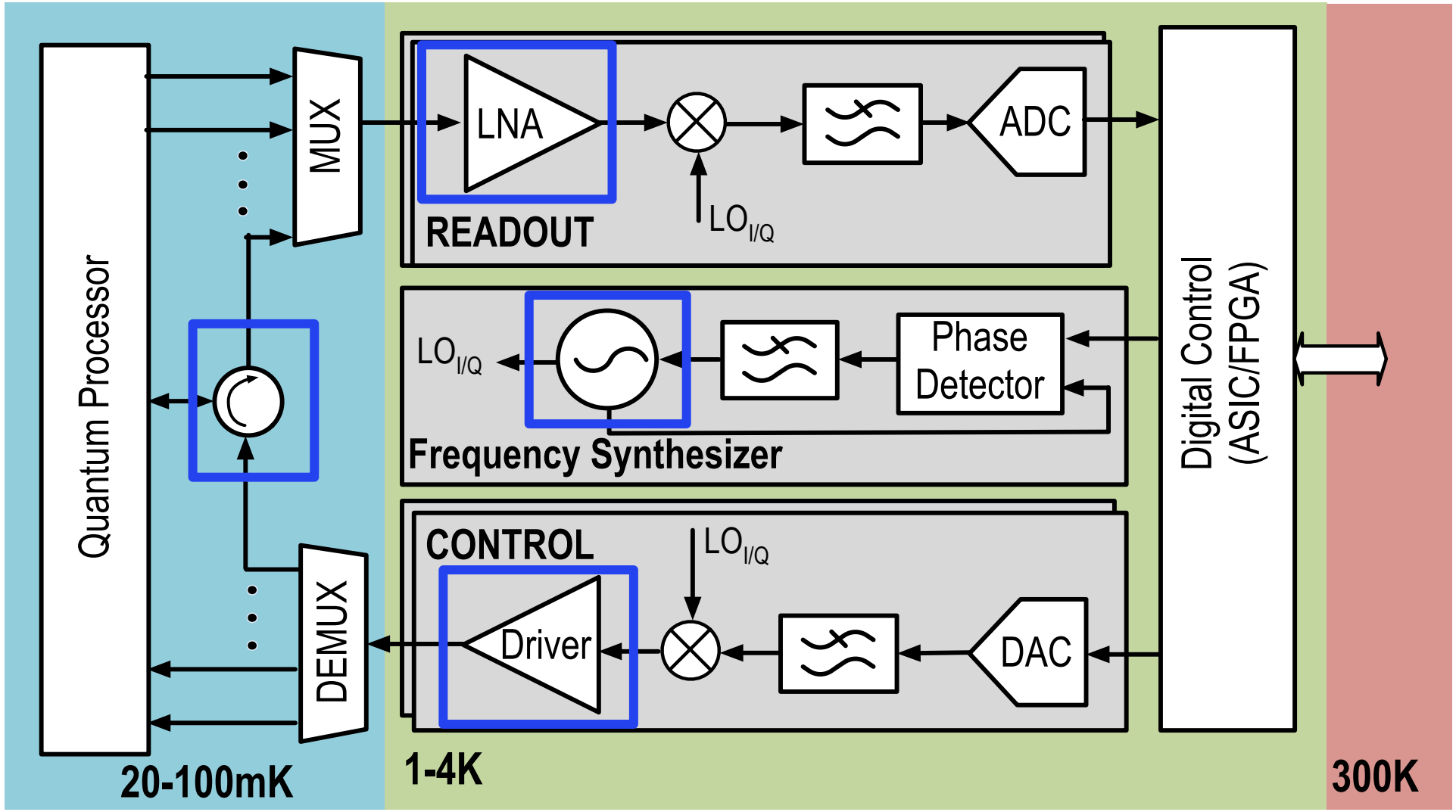
State-of-the-art quantum computer (53 qubits)



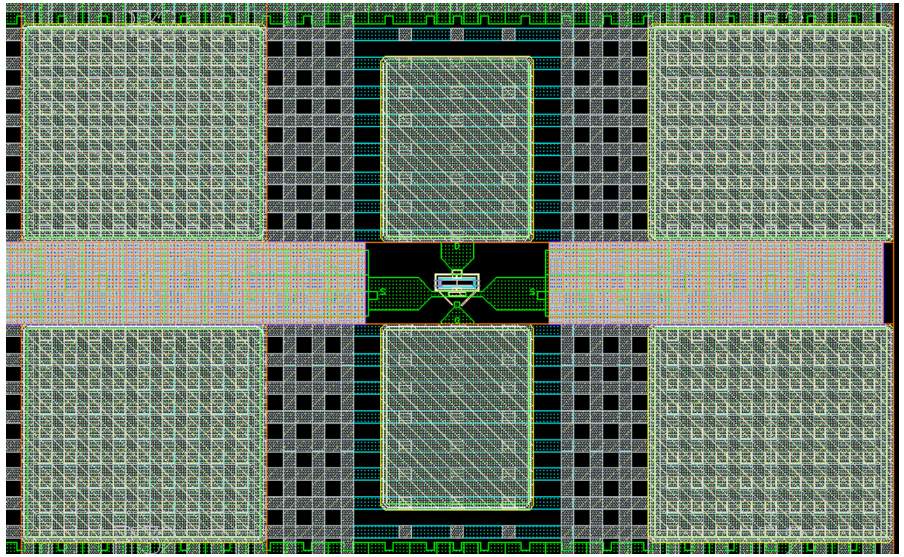
[Bardin, 2019]

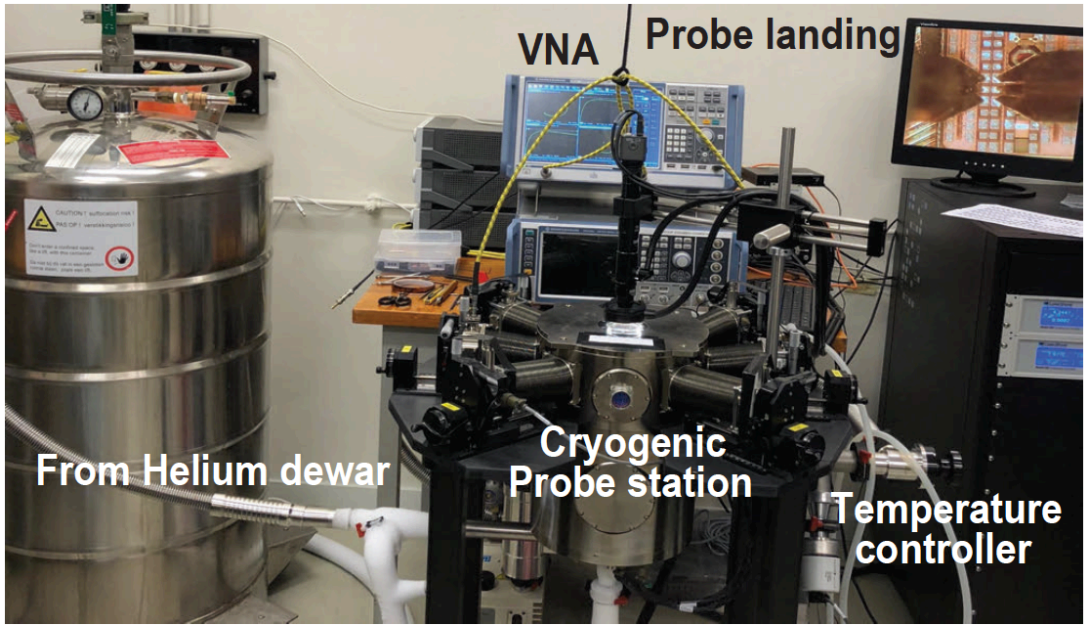


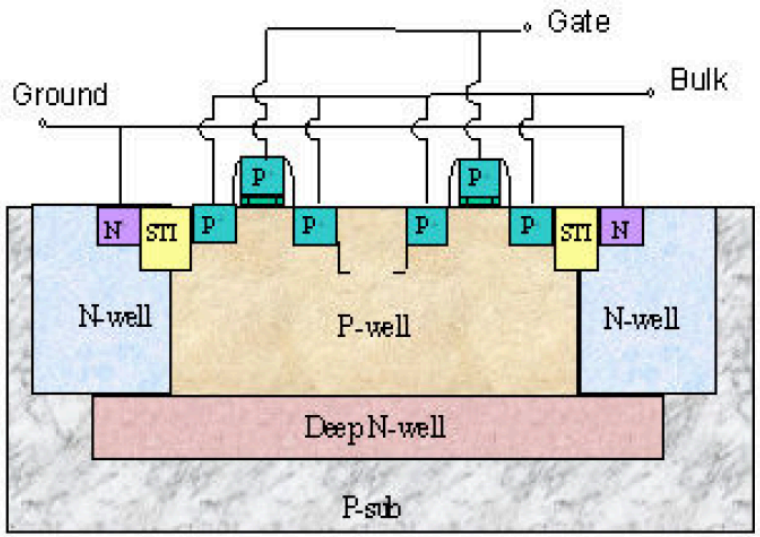
A Scalable Quantum Computer

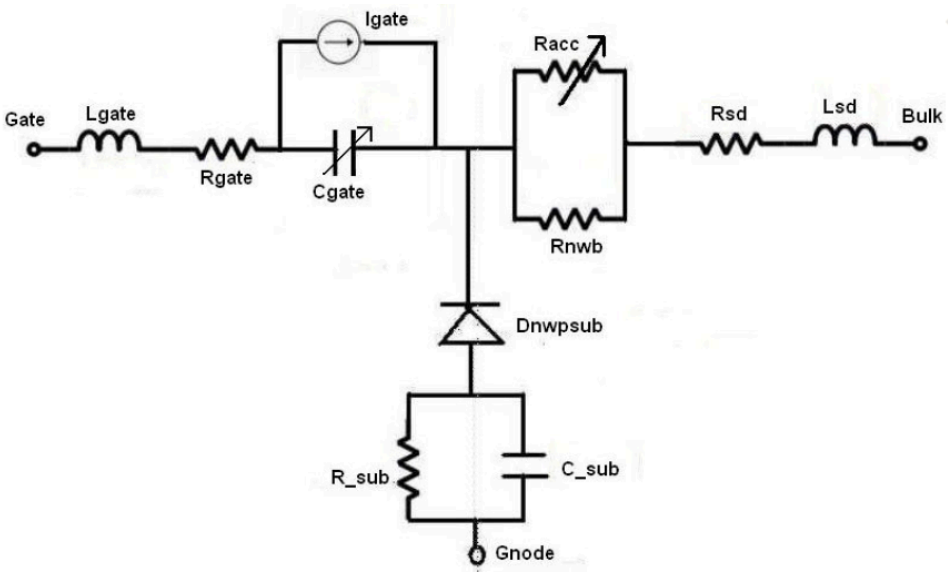


Project-1: Characterization and Modeling of Transistors/Varactors









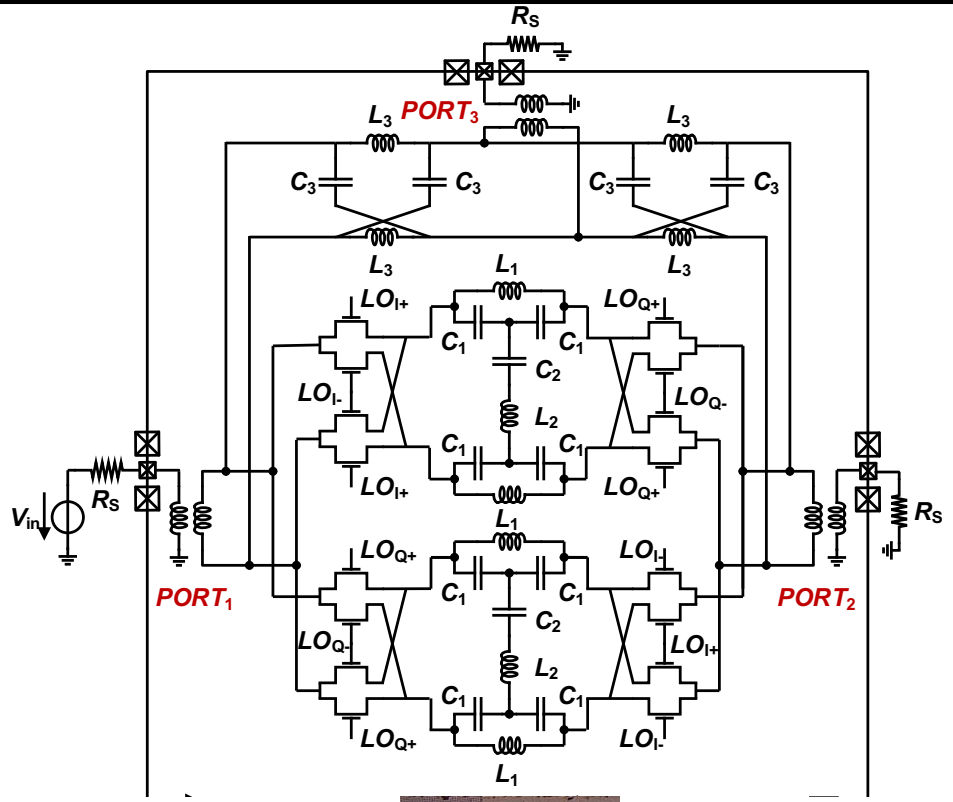
Collaboration with Dr. Spirito

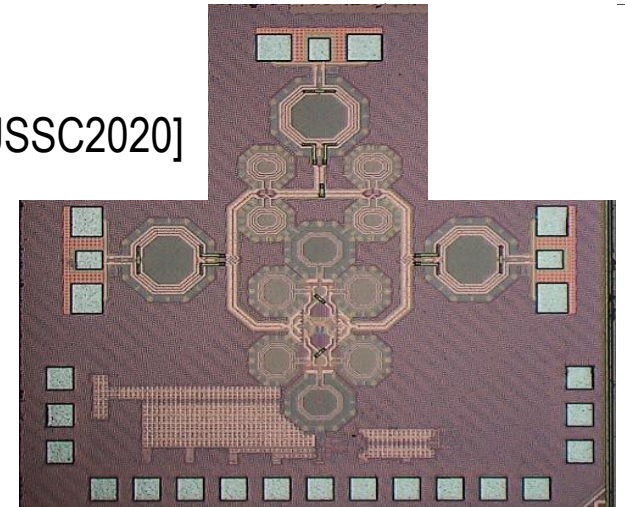
Project-2: Design of a Cryogenic Isolator for Quantum Computers

Magnetic materials

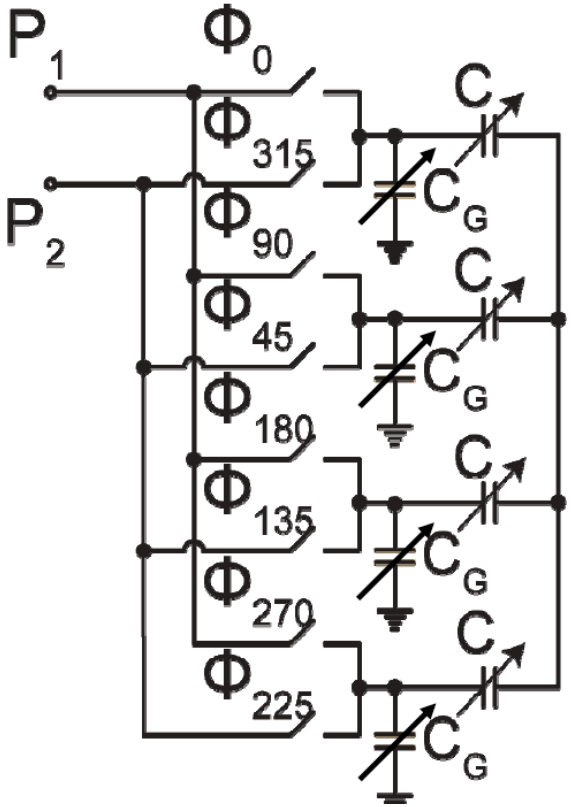
QuinStar Technology Inc.

- Bulky
- CMOS incompatible



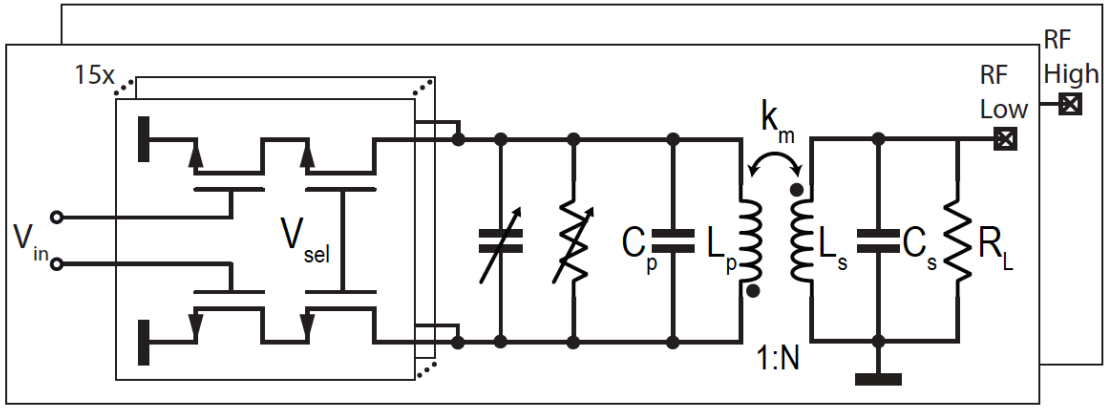


[A. Ruffino, JSSC2020]



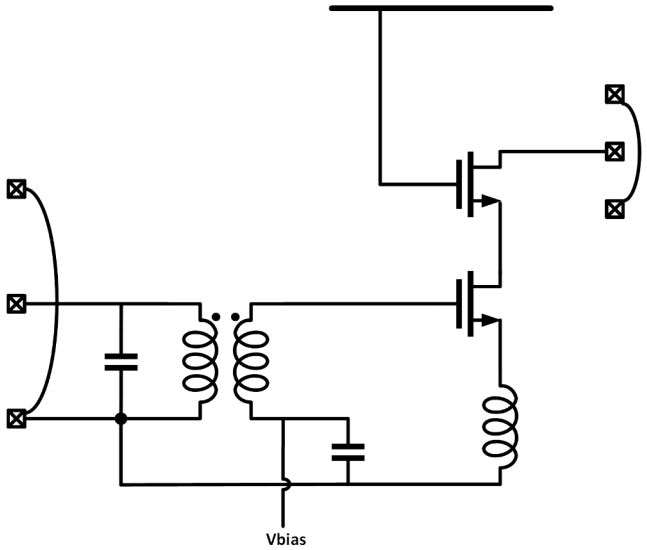
- **Specifications**
  - Process: 22/40-nm CMOS
  - Tape-out date: Q1/Q3 2021
  - BW: 6-8 GHz
  - NF/Insertion loss: 1 dB
  - Isolation: >20 dB

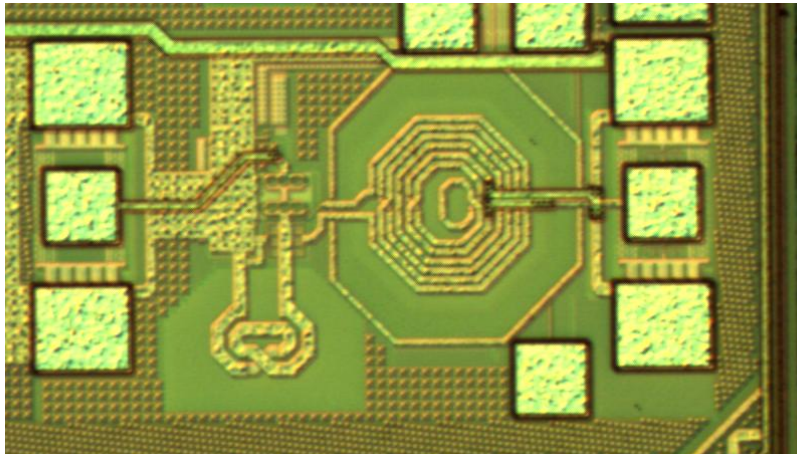
Project-3: Design of a Linear Wideband Class-F Power Amplifier



- **Specifications**
  - Process: 22/40-nm CMOS
  - Tape-out date: Q1/Q3 2021
  - BW: 6-20 GHz
  - Linearity (IM3): 50 dBc
  - Output power: >0 dBm
  - Class-F or F^{-1} operation

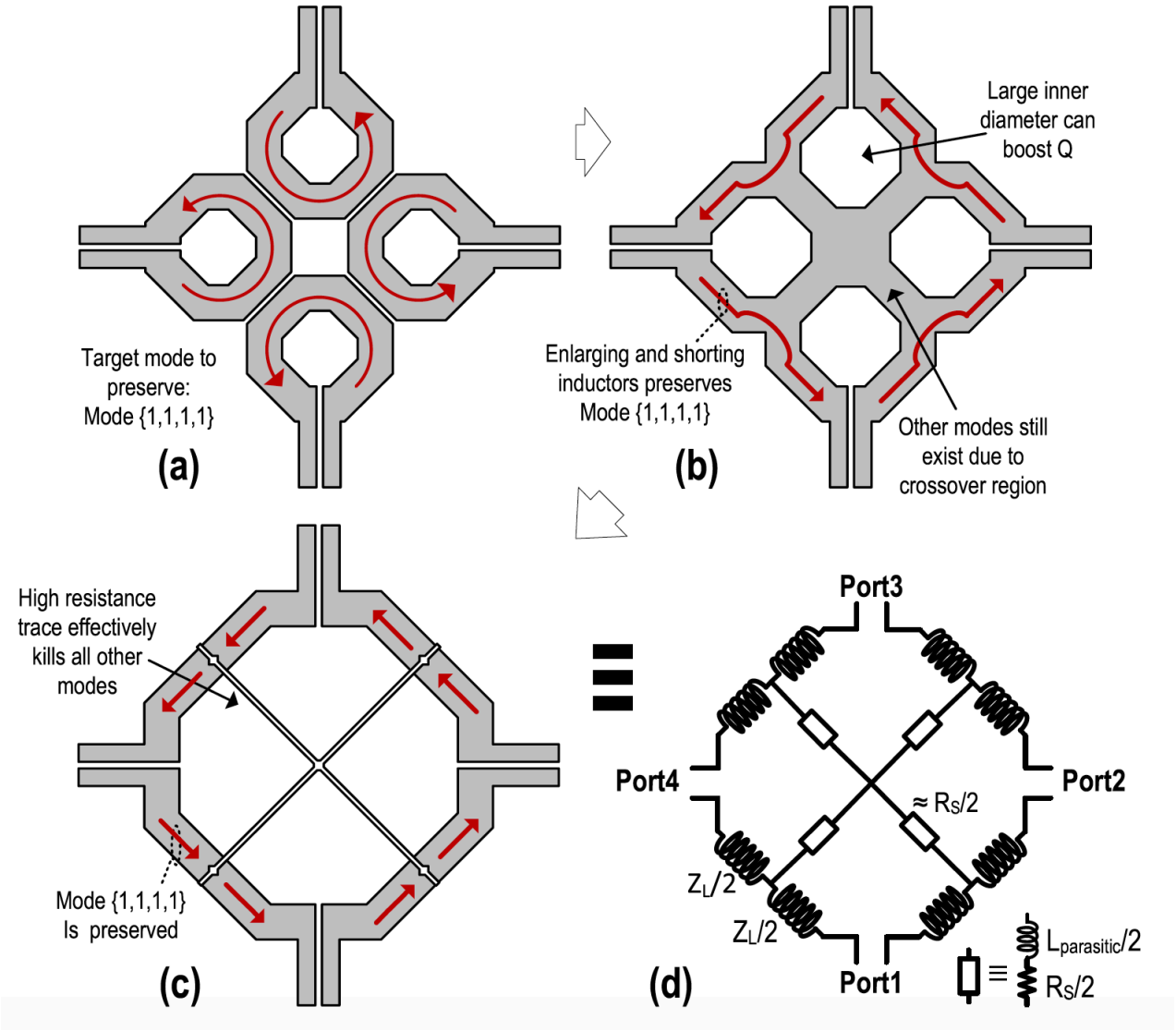
Project-4: Design of a Wideband Low Noise Amplifier



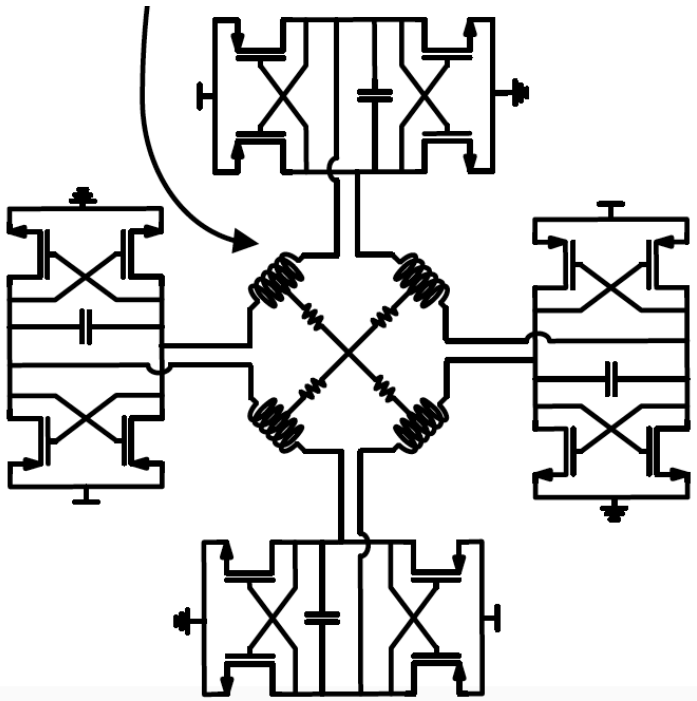


- **Specifications**
  - Process: 22/40-nm CMOS
  - Tape-out date: Q1/Q3 2021
  - BW: 6-8 GHz
  - Noise figure < 0.15dB

Project-5: Design of an Ultra-Low Phase Noise Oscillator

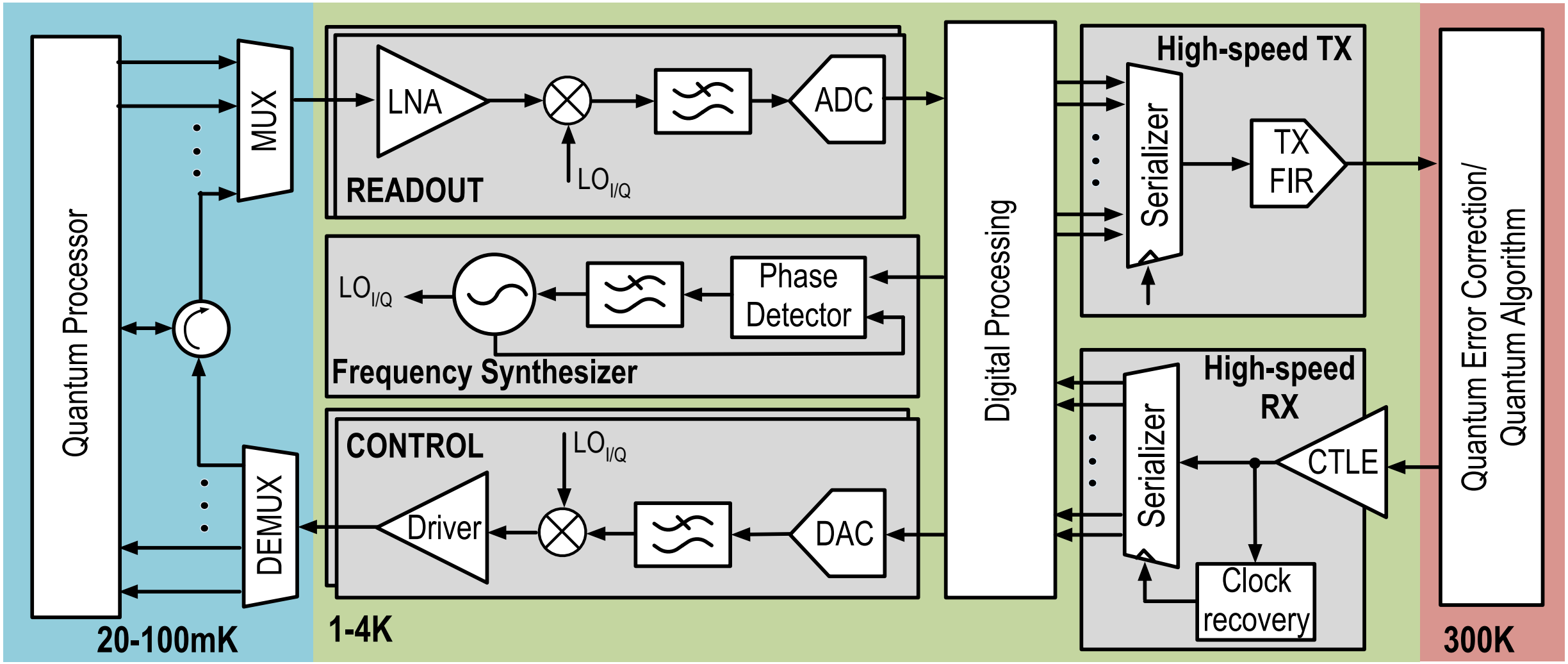


- **Specifications**
  - Process: 22/40-nm CMOS
  - Tape-out date: Q1/Q3 2021
  - Freq: 10-20GHz
  - Phase noise < -150dBc/Hz @3MHz offset frequency

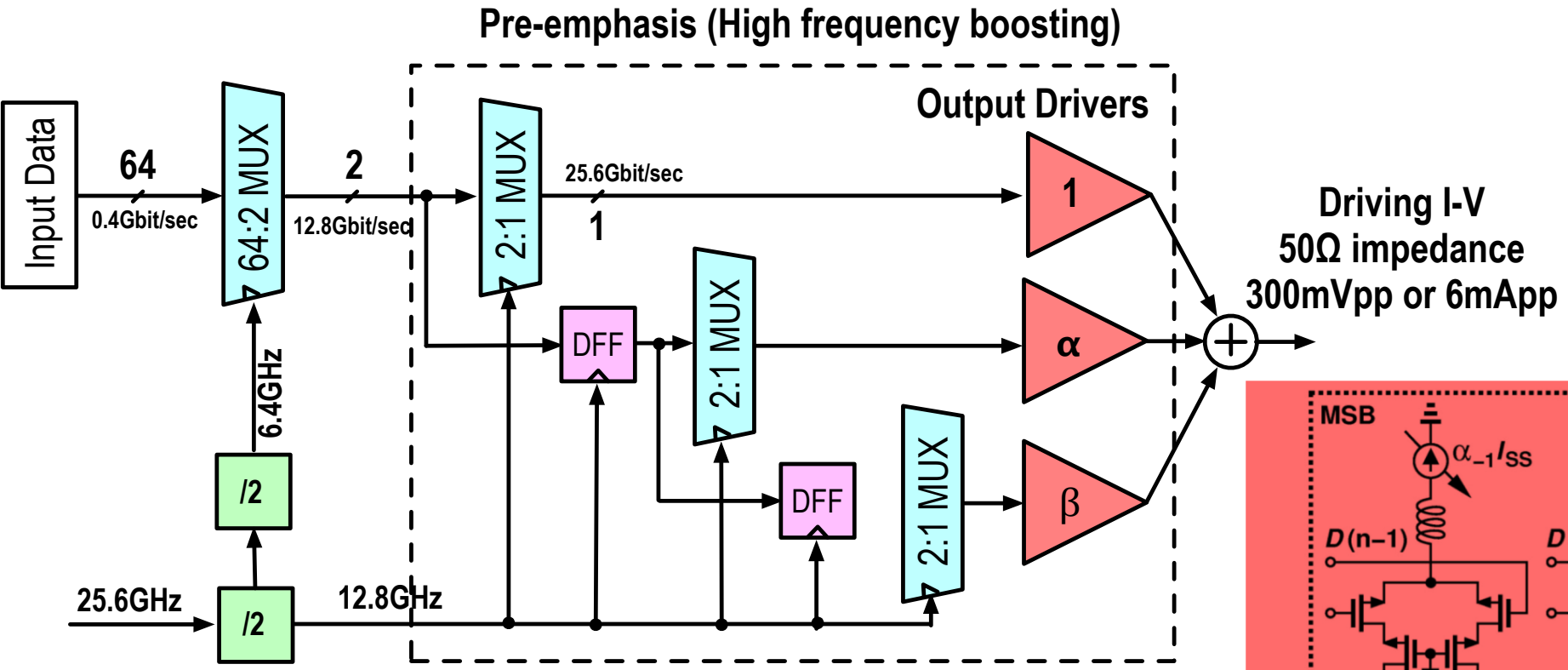


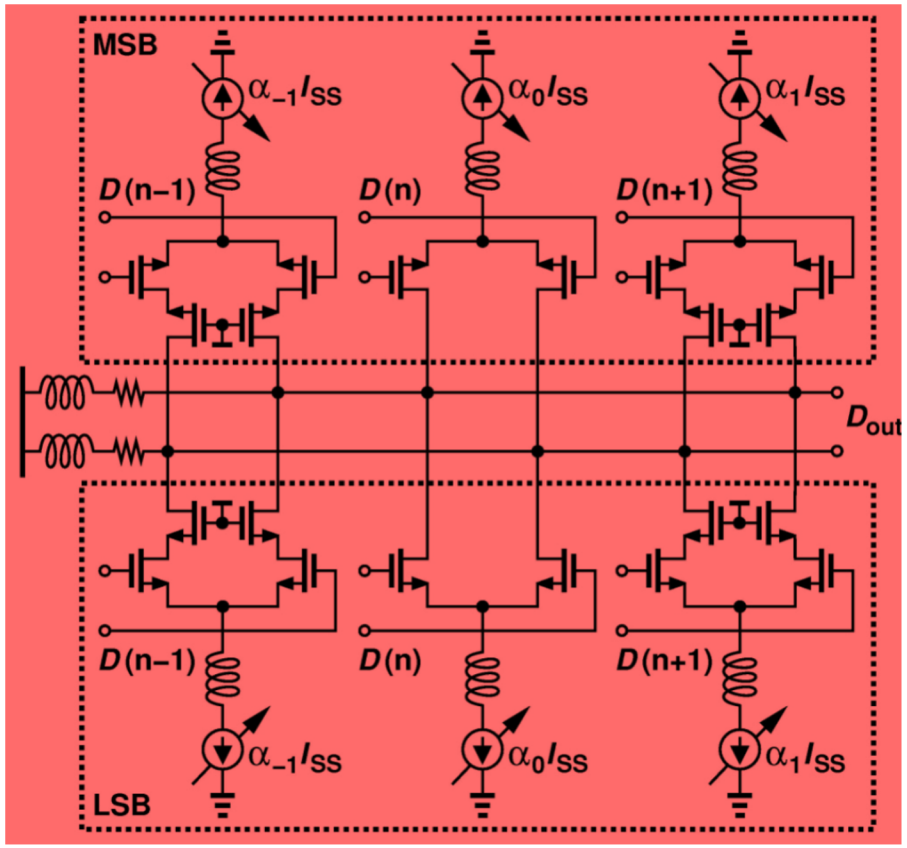
Cryogenic High-Speed Link

Need for Cryogenic High-Speed Wireline Link



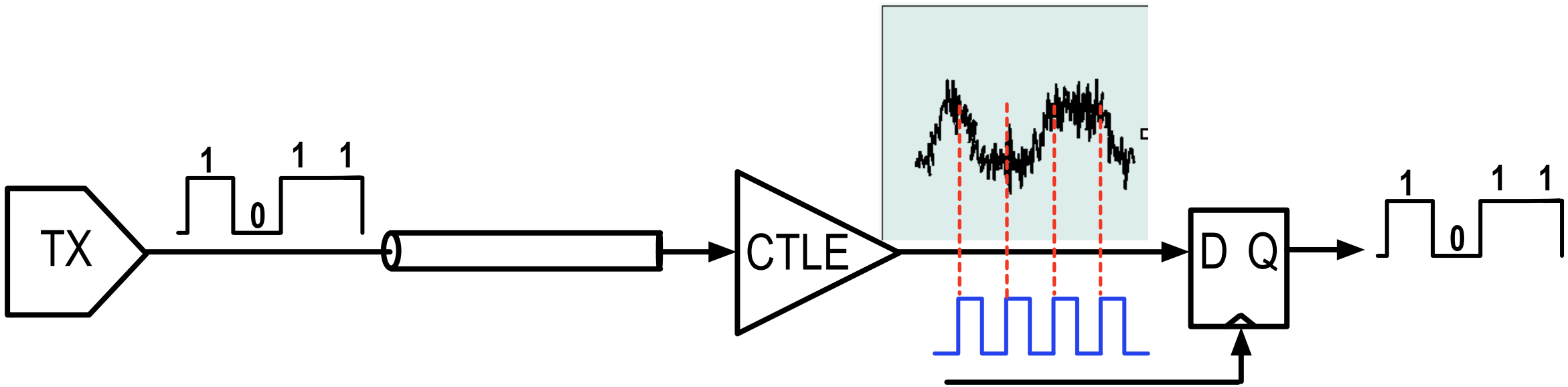
Project-6: Need for Cryogenic High-Speed Wireline Transmitter



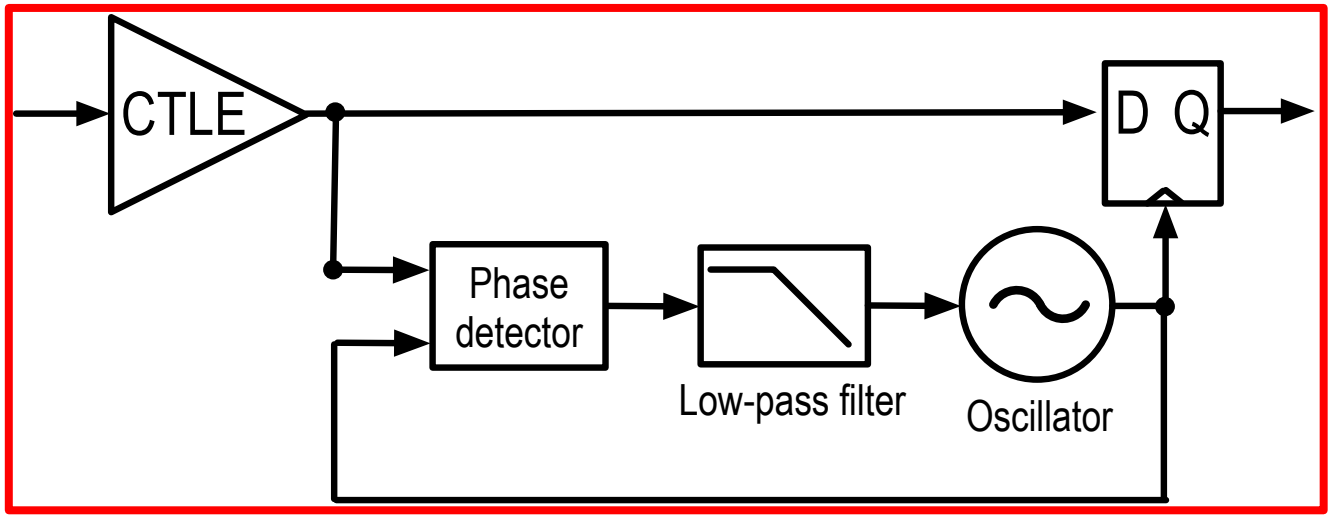


- **Specifications**
  - Process: 22 FinFet Technology
  - Tape-out date: Q1/Q3 2021
  - BW: 40 GHz
  - PAM-4

Project-7: Clock and Data Recovery (Cryogenic PLL)



- **Specifications**
  - Process: 22 FinFet Technology
  - Tape-out date: Q1/Q3 2021
  - Freq: 25 GHz
  - Jitter < 100fsec
  - Power consumption < 5mW



Cryogenic Broadband Amplifier and TDC for Readout of Superconducting Nanowire Single Photon Detector

Collaboration with
Dr. Sebastiano

Readout Circuit for Superconducting Nanowire Single Photon Detectors

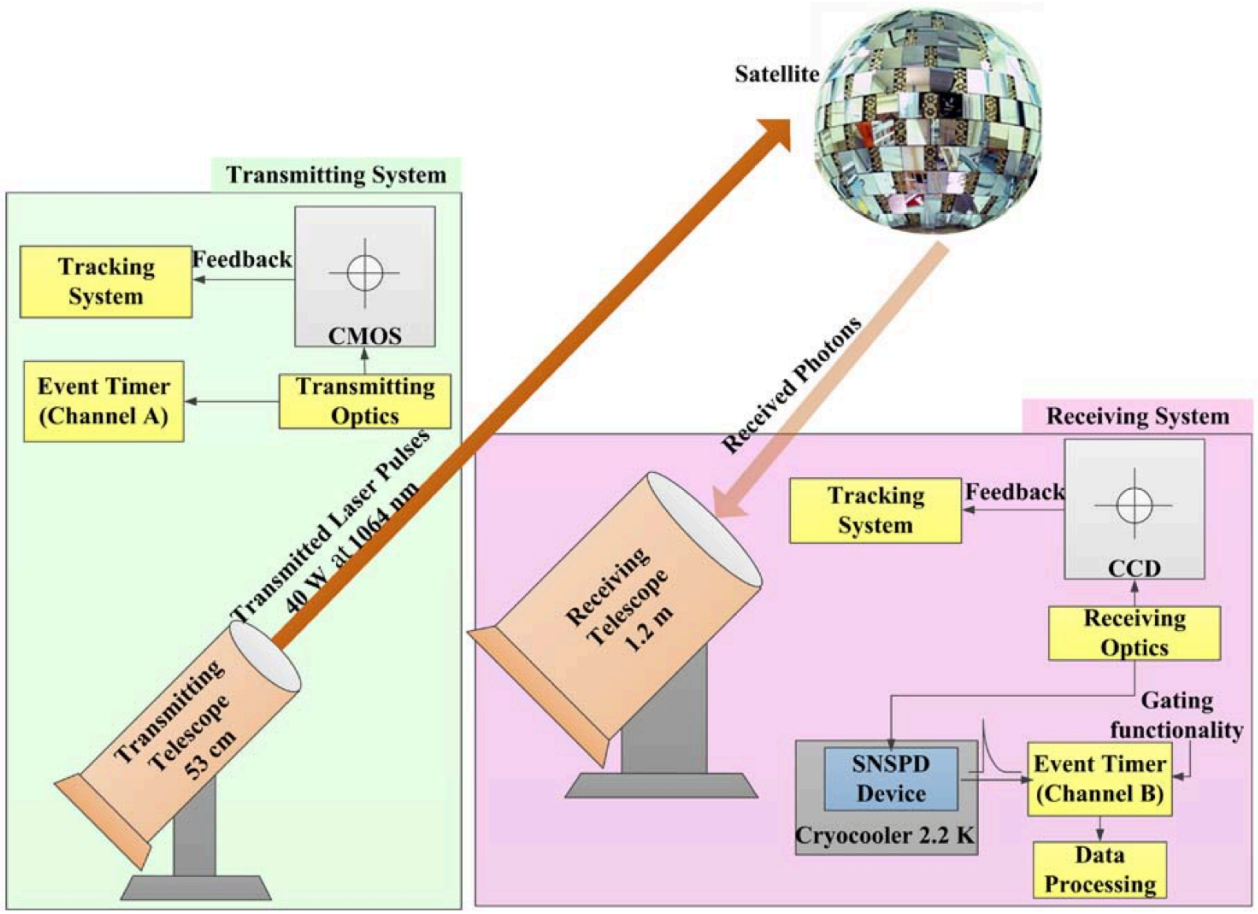
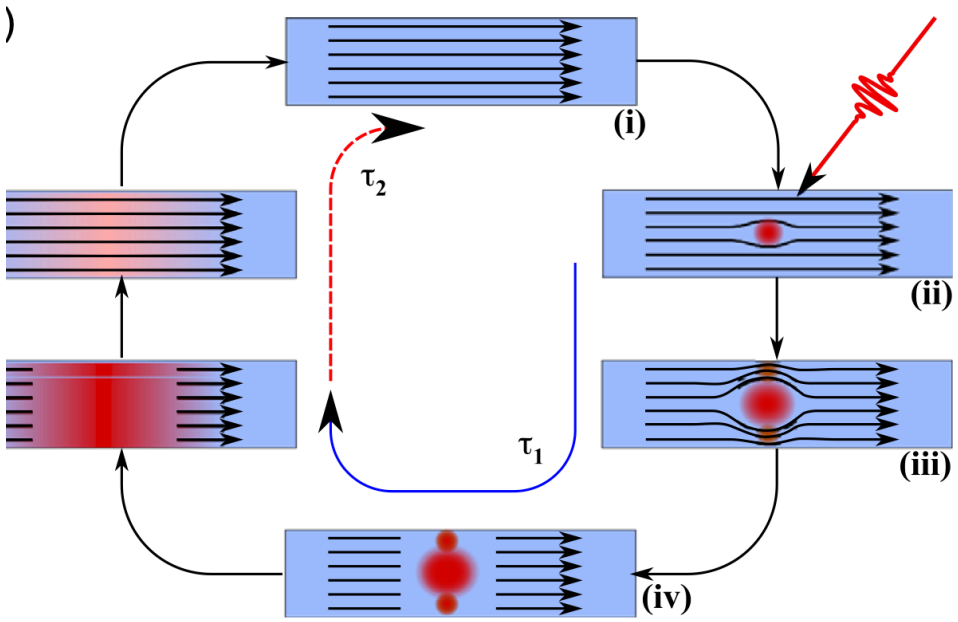
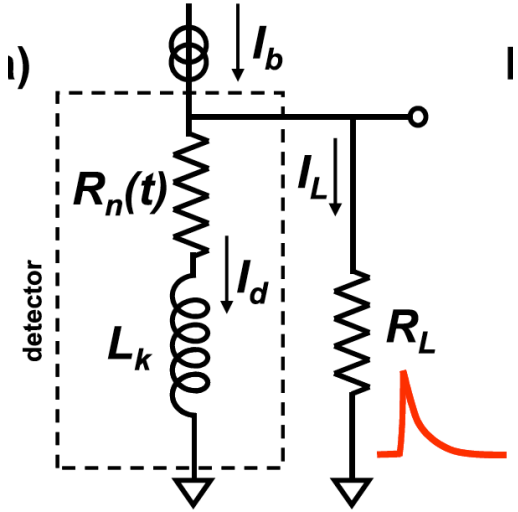
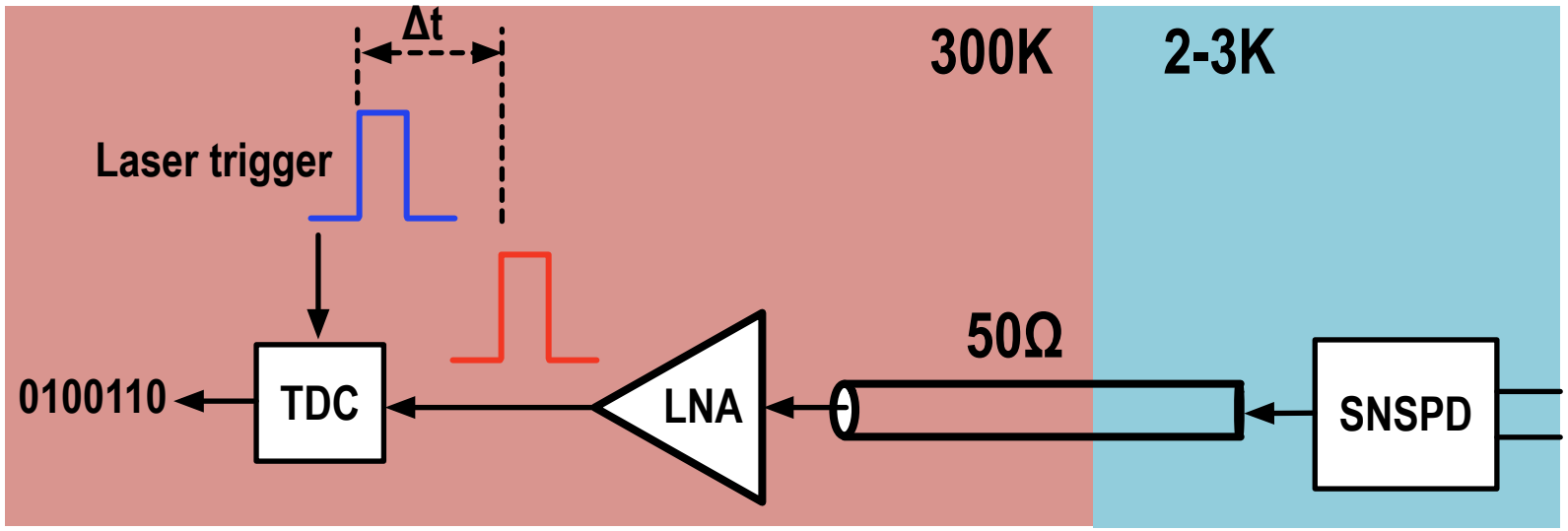


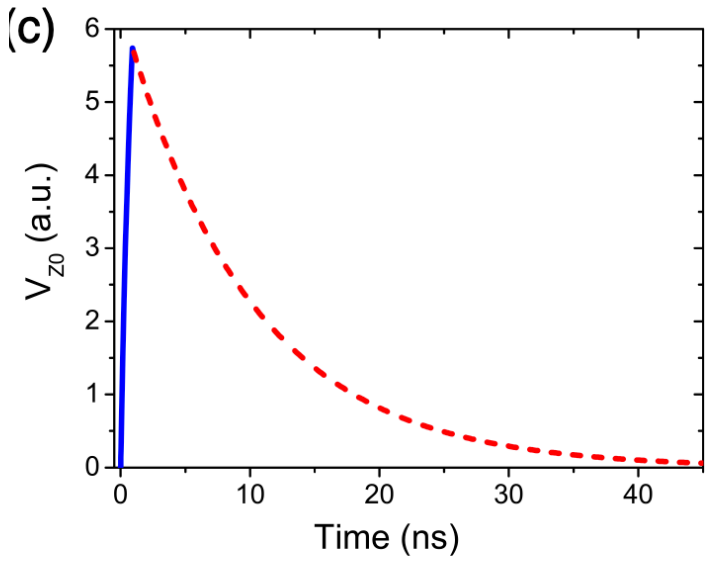
Fig. 1. Experimental setups for SLR using the SNSPD. Laser pulses were transmitted through one telescope, and the echoes from the satellites were coupled to the SNSPD device through the other telescope.

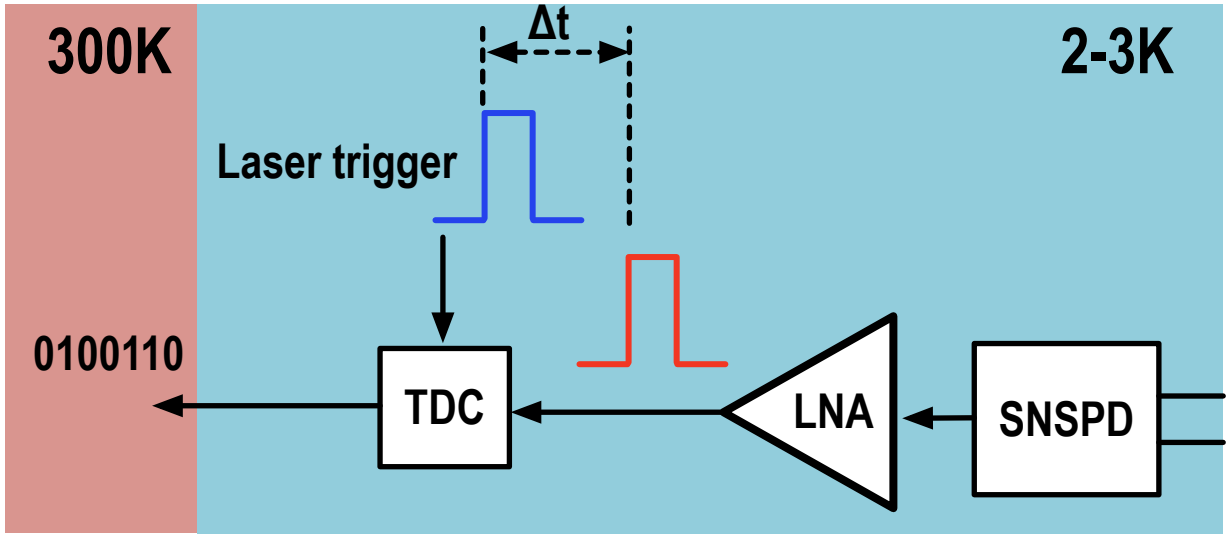




Readout Circuit for Superconducting Nanowire Single Photon Detectors







- **Project. 8:**
  - Design of a cryogenic broadband Amplifier
- **Project. 9:**
  - Design of a cryogenic time-to-digital (TDC) converter