



SURF

Experimental Technologies Platform

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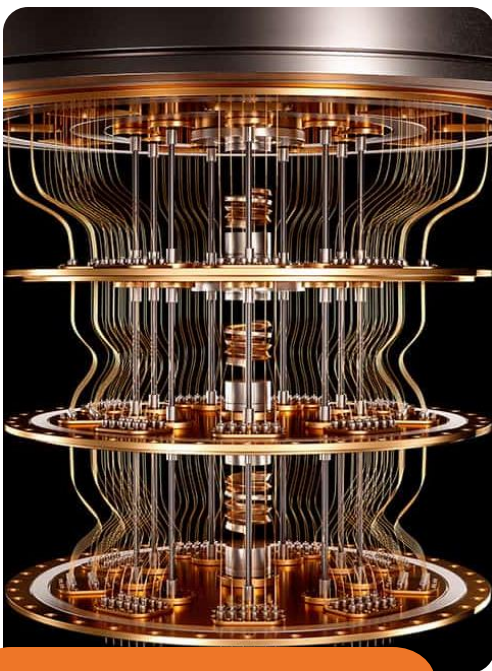
11 December, 2024

AMBITIE

**SURF is committed to actively facing
future challenges in the field of
scientific research and computing**

| Tomorrow's challenges

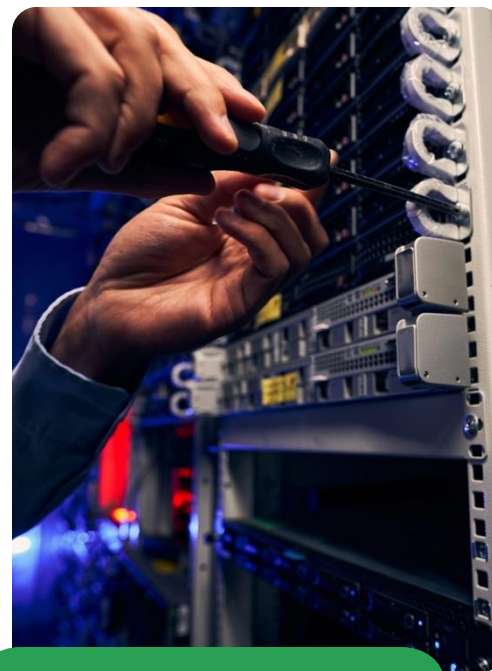
As technology evolves and research demands grow, **we face critical challenges in staying ahead**, from managing vast data ecosystems to scaling sustainable infrastructure and fostering seamless collaboration.



Evolving technological landscape



Growing demand for data processing



Scaling infrastructure



Fostering interoperability

| Experimental platforms

Experimental platforms enable exploring, testing, and refining new technologies and methodologies, ensuring readiness for future demands in research and infrastructure development.



Knowledge

Installing, configuring, and maintaining experimental software or hardware requires continuously updated expertise.



Access

Access to experimental technologies is often hindered by economic, legal, and bureaucratic complexities.



Efficiency

Exploration and assessment tasks normally result in low utilization ratios per project, limiting overall impact.

| SURF-ETP

SURF Experimental Technologies Platform

Fosters an open and collaborative innovation ecosystem, bringing together researchers, system engineers, and experimental hardware infrastructures to facilitate the assessment of cutting-edge ICT technologies and methodologies.

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| SURF-ETP

Projects

Bring domain knowledge and pose challenges and questions to be solved.

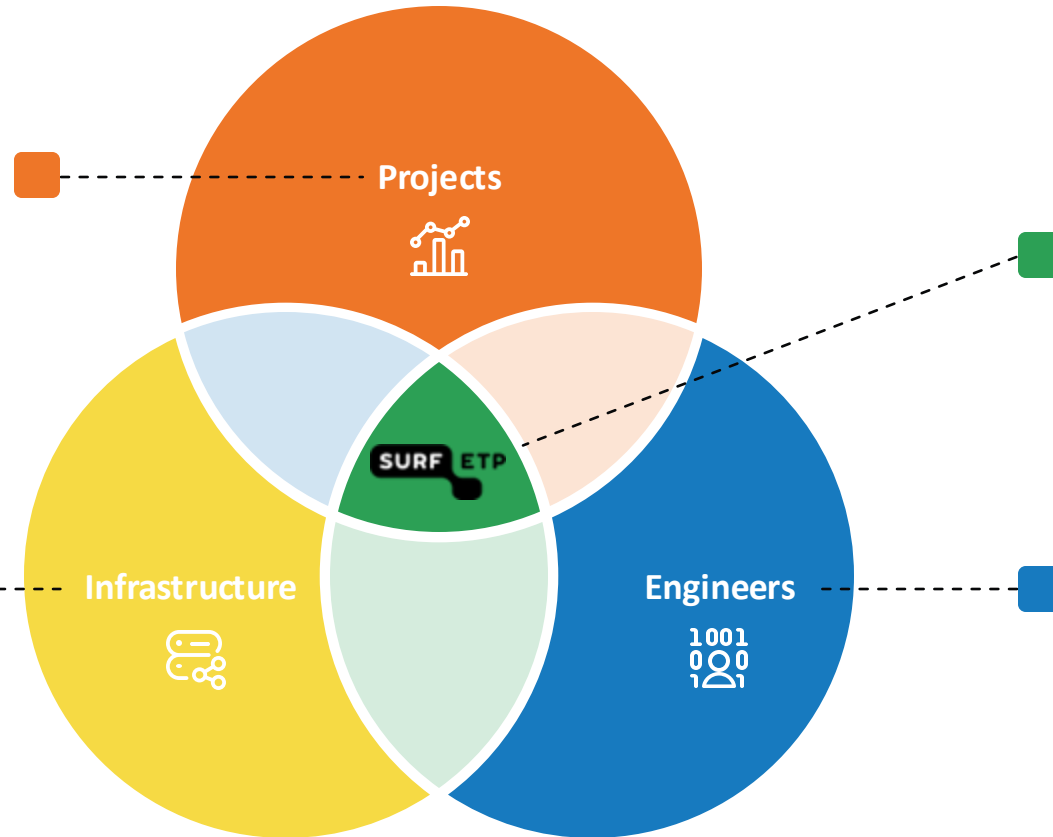


Infrastructure

Evolves continuously, adapting to the needs of future research problems.



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SURF-ETP

Open and collaborative environment to foster the assessment of cutting-edge technologies and methodologies.

Engineers

Leverage their technical skills and motivation to surf the state-of-the-art.

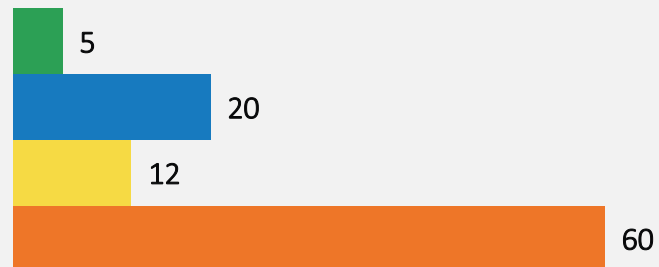


| SURF-ETP in numbers

Events
Organization of
bootcamps or
workshops



Projects
Technology
assessment or
development



■ Events ■ Projects ■ Members ■ Users



Members
SURF members
accessing the
platform



Users
Total number of
users accessing the
platform

Dutch members

UNIVERSITY
OF TWENTE.

TU Delft

TNO innovation
for life

Erasmus MC
Universitair Medisch Centrum Rotterdam

WAGENINGEN
UNIVERSITY & RESEARCH

university of
 groningen



netherlands
eScience center

Nikhef



Amsterdam UMC

ASTRON

SURF



Events



Future Computing and Networking

FIRE (FPGA Innovation Research Exchange) - Second Edition

On December 6th, 2023, SURF in Utrecht successfully organized the second edition of FIRE FPGA symposium along with the acceleration community. This is the continuation of the Innovation Research Exchange event series. The focus was on application development using HW-SW co-design. The event addressed the challenge of optimizing applications on heterogeneous CPU-accelerator systems to achieve full system optimization.

We had a number of speakers from industry, academia and research institutes. In addition, we organized a session with 5-minute presentations, where many researchers and companies presented innovations and products at a high pace to encourage collaboration and information exchange.

07 februari 2024

645

Leestijd 5 minuten

0 [Praat mee](#)

[Volgen](#)

Lat



Future Computing and Networking

FIRE (FPGA Innovation Research Exchange) - Third Edition

On June 27th, 2024, SURF along with Dutch Hardware Acceleration network organized the third edition of FIRE (FPGA Innovation Exchange) workshop. The theme of this edition was about hardware acceleration for AI workloads.

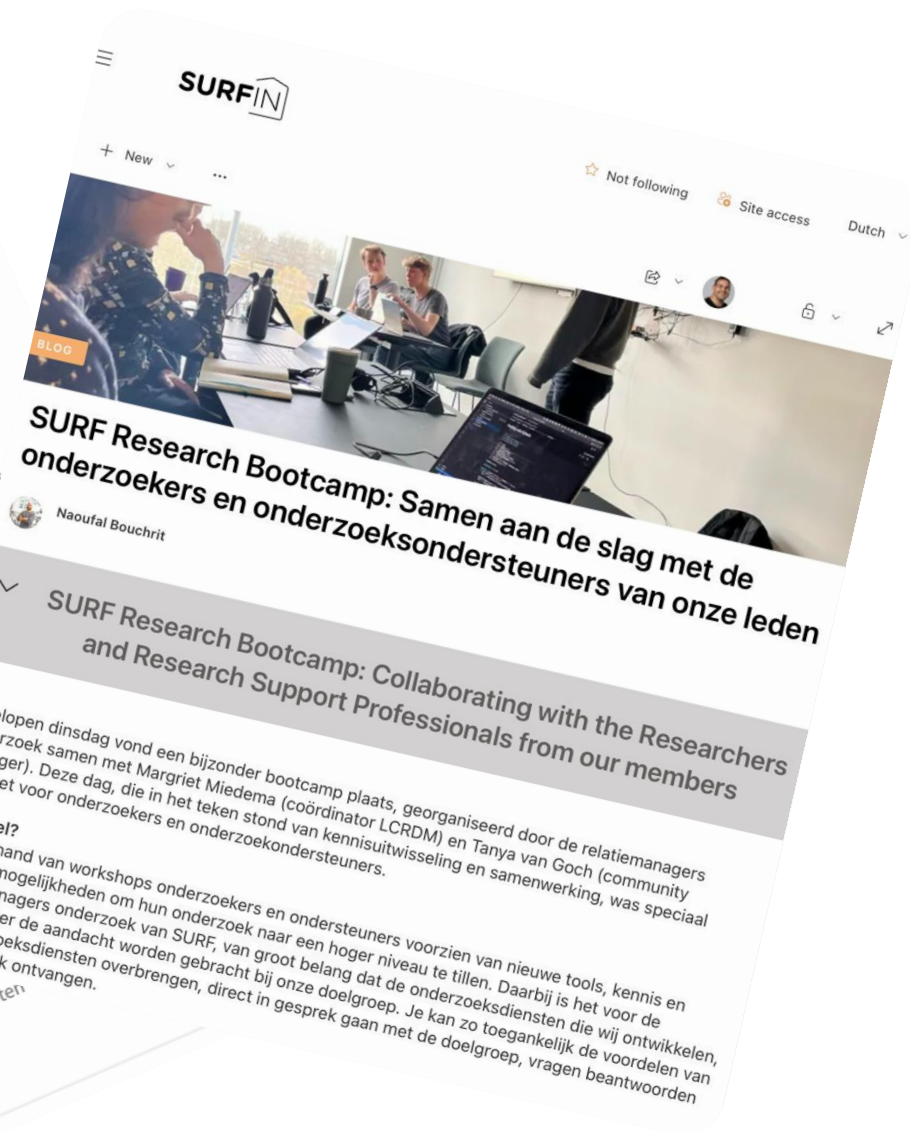
The event featured a lineup of discussions centered around edge computing technologies such as Innatera and multiple industrial players for AI workload acceleration. In addition, the workshop featured two keynote developers of HW acceleration platforms such as platforms dedicated to quantum computing and automata.

21 oktober 2024

231

Leestijd 5 minuten

[Volgen](#)



Partnerships and collaborations



| Infrastructure

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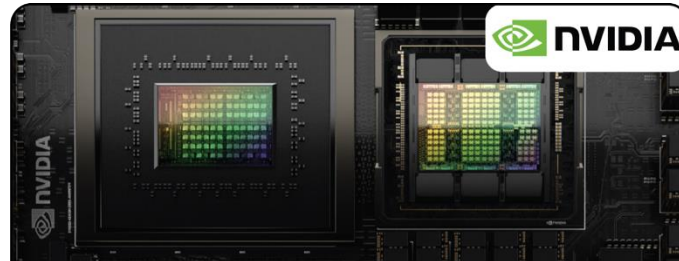
| Available technologies

Compute and data processing



Intel GPU Max 1100

Designed to accelerate AI workloads and enable vector and matrix capabilities with Intel Xe Matrix Extensions (XMX).



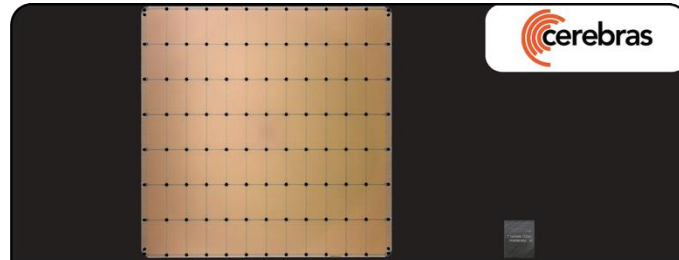
NVIDIA Grace Hopper Superchip

NVIDIA GH200 combines the Grace and Hopper architectures via NVLink-C2C to deliver a CPU+GPU coherent memory model.



AMD Instinct MI210

AMD Instinct MI210 accelerators power enterprise, research, and academic HPC and AI workloads for single-server solutions and more.



Cerebras WSE-2

850,000 cores, 40 GB of on-chip SRAM, 20 PB/s of memory bandwidth, and 220 Pbps of interconnect bandwidth.

| Available technologies

Compute and data processing



Asus CRL-G116U-P3DF

AI accelerator card based on Google Coral Edge TPU processor, enabling AI-based real-time decision process at edge.



NextSilicon Maverick

Intelligently adapts its architecture to meet algorithmic requirements, all without the need for code modifications.



Xilinx ALVEO U250

The Alveo U250 card uses Xilinx SSI technology to deliver breakthrough FPGA capacity, bandwidth, and power efficiency.



Xilinx VCK5000 Versal

The VCK5000 Versal is built on the AMD 7nm adaptive SoC architecture and is designed for (AI) Engine development with Vitis end-to-end flow and AI Inference development.

| Available technologies

Network, storage, and infrastructure



Cornelis Omni-Path Express

Cornelis Omni-Path Express is the next generation of high performance fabrics, a proven hardware foundation combined with the OpenFabrics Interfaces (OFI) software framework.



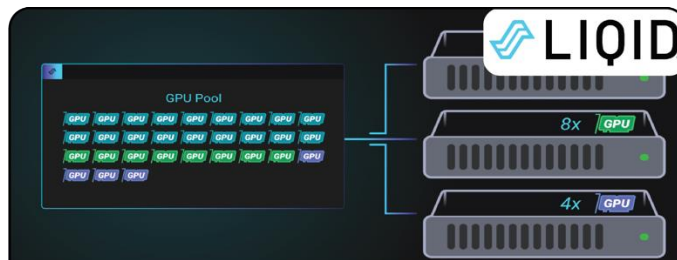
Nokia 7750 SR-1x-48D

The Nokia 7750 Service Router (SR) portfolio delivers unrivalled performance, scale and versatility for the full array of IP edge and core applications.



Fungible FS1600

The FS1600 is powered by two Fungible DPUs, a new class of microprocessors designed to deliver unrivalled performance and efficiency in running infrastructure services.



Liquid Composable Infrastructure

Liquid GPU On-Demand allows you to provision, scale and migrate GPUs via software to satisfy your most challenging workloads.

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| Projects

IgANet—Physics-informed isogeometric analysis NN

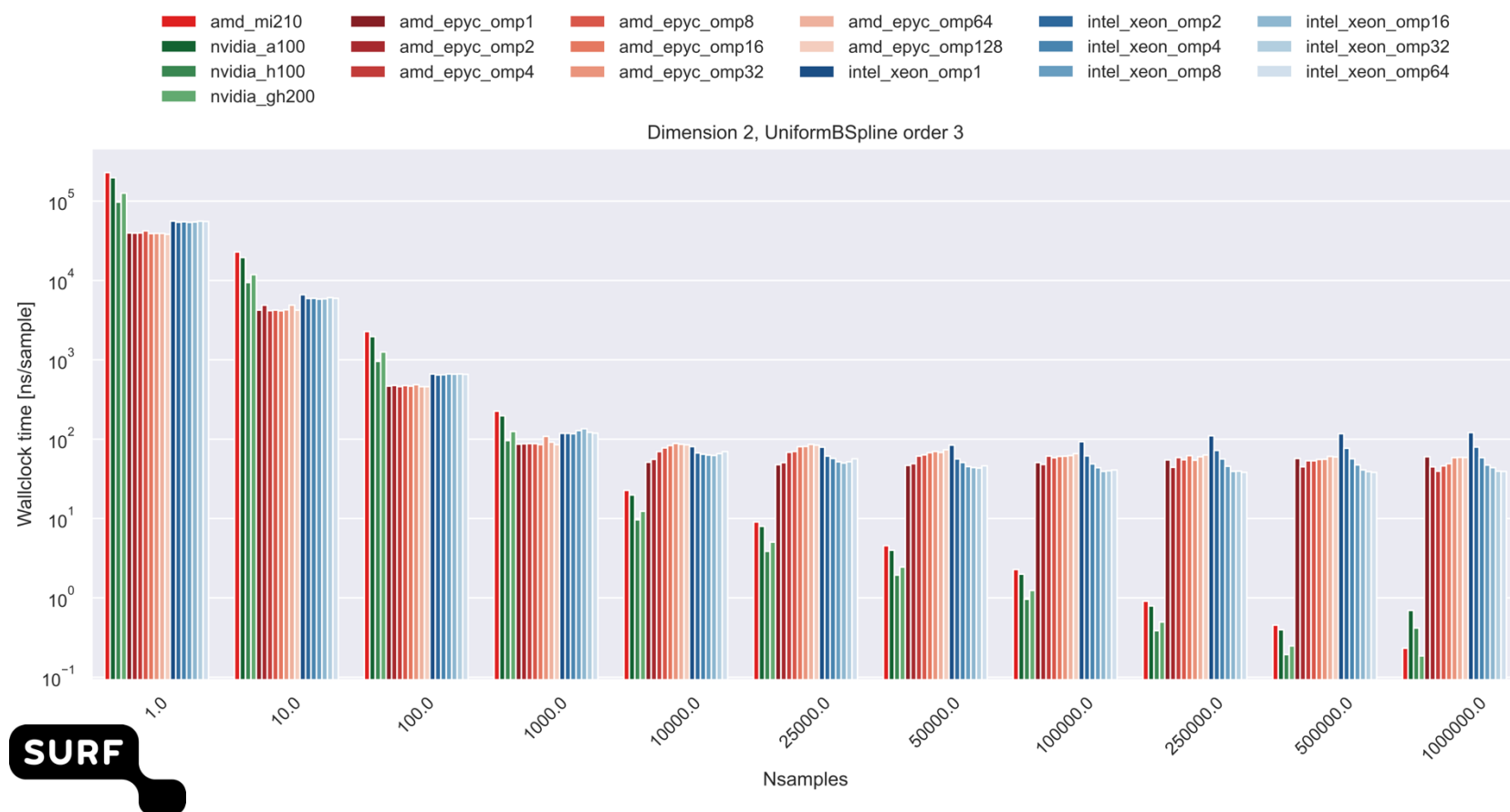
Project Nr	SURF participants	Partners
SURF-ETP-0001	Bas (HPCV), Yue (HPML), Xavier (HPCV)	Matthias (TU Delft)

Summary

IgANet is a new type of physics-informed deep operator learning approach that enables interactive design-through-analysis workflows by combining the strengths of isogeometric analysis (e.g., accurate and user-friendly geometry modelling using splines) and SciML (ultra-fast response times).

Highlights

- Gained access to AMD GPU platforms with ROCm toolchains.
- Upgraded the Cmake scripts to adapt the builds to the MI210 platform.
- Disseminated the performance results shown in multiple talks.



Quantum–HPC hybrid system interaction

Project Nr	SURF participants	Partners
SURF-ETP-0003	Ariana (Labs), Bas (HPCV), Jaap (HPCV)	QuTech, Richard (TNO), Christiaan (TNO), Olaf (TU Delft)

Summary

We are in a crucial moment to further develop our knowledge and understanding of **quantum computing** and its applications.

This project aims to support QuTech demonstrators with SURF supercomputing capabilities, develop hybrid quantum computations, orchestrate quantum networks, and pursue collaboration to **strengthen the Netherlands' leadership** in quantum technologies.

Highlights

- Installed dependencies on ETP servers for the integration with Quantum Inspire.
- Investigated options for global installation such as creating an easy build.
- Collaborated with Ariana Torres to test job submissions and queries using tokens.



| Evaluation of Cerebras CS-2 WSE

Project Nr	SURF participants	Partners
SURF-ETP-0004	Duncan (HPML), Mohsen (HPCV), Xavier (HPCV)	Cerebras

Summary

Cerebras Systems' CS-2 WSE is a purpose-built system designed to accelerate scientific computing and AI workflows. As such, it delivers the wall-clock compute performance of tens to hundreds of GPUs on specific workloads. To comprehend such unconventional hardware, SURF partnered with Cerebras to conduct a technology assessment.

Highlights

- Investigated the Cerebras documentation and SDK.
- Executed a set of AI workflows.
- Partnered with a cutting-edge hardware vendor, Cerebras, with the ultimate goal of facilitating access to Cerebras systems for Dutch researchers in the future.



Optimization of data pipelines in radio astronomy

Project Nr	SURF participants	Partners
SURF-ETP-0006	Duncan (HPML), Raymond (DDP), Mohsen (HPCV), Bas (HPCV), Jaap (HPCV)	Steven (ASTRON), Victor (ASTRON), Nikolaos (Twente)

Summary

This project explores the use of Xilinx Adaptive Compute Acceleration Platform (ACAP) for advancing signal processing in radio astronomy at ASTRON, the Netherlands Institute for Radio Astronomy. It focuses on leveraging ACAP's capabilities to improve workflows for large-scale data processing and real-time analytics. By integrating ACAP into existing systems, the project aims to enhance efficiency, flexibility, and energy efficiency, supporting the continued advancement of radio astronomy research.

Highlights

- Gained access to Xilinx ACAP platforms.
- Established a configuration procedure ensuring a complete software ecosystem for FPGAs.
- Evaluated the use of Versal Adaptive SoC for efficient signal processing in radio telescopes.



WiLLMa

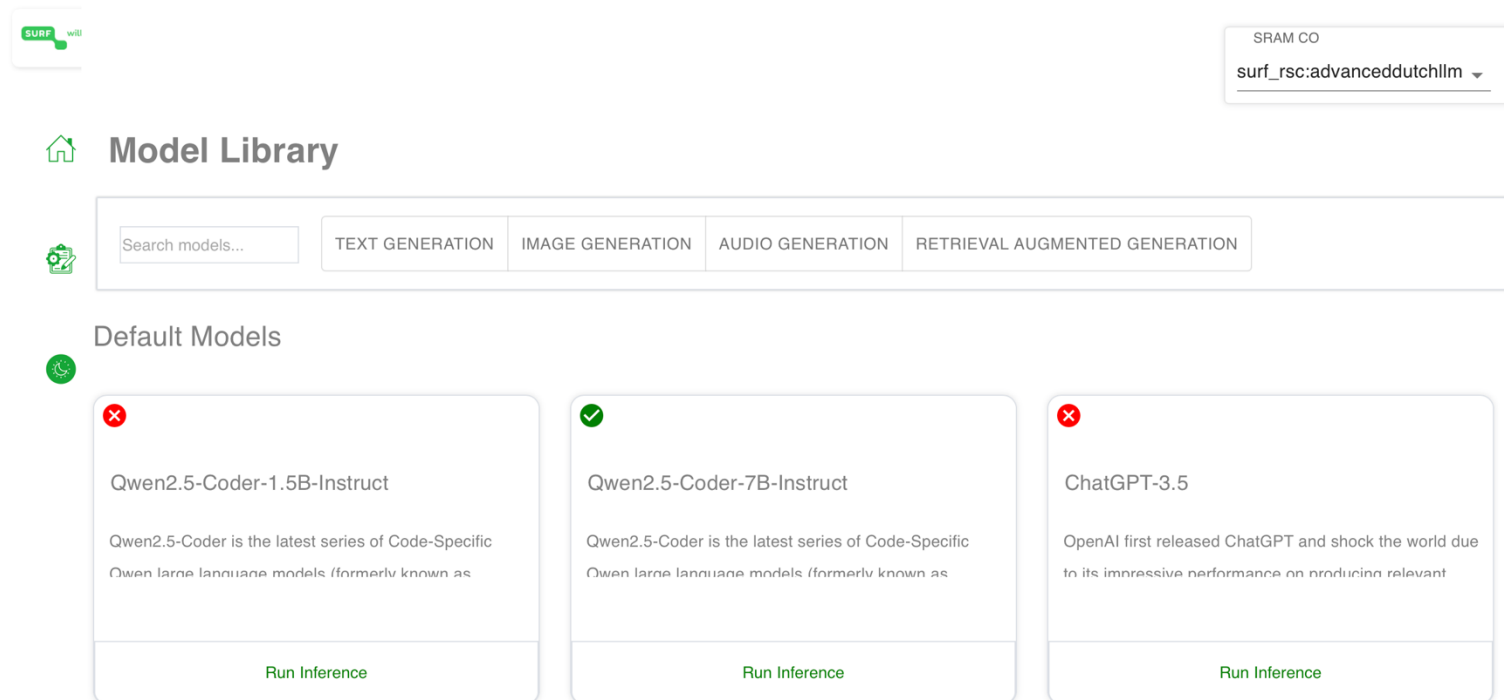
Project Nr	SURF participants
SURF-ETP-0018	Damian (HPML), Duncan (HPML), Thomas (HPCV), Jaap (HPCV), Bas (HPCV)

Summary

WiLLMa aims to develop an infrastructure to facilitate hosting and provisioning of various LLMs to our community. The project aims to create a centralized platform where users can access a diverse range of LLMs for their specific needs.

ETP contribution


- Managed a hosting setup of exclusive GPU nodes with NVMe for LLM inference.
- Configured reverse proxy forwarding for accessing stable and development platforms.
- Deployed SSH certificates for secure HTTPS communication.
- Established user accounts with appropriate permissions for secure service management.




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**Thank you for
your attention!**

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