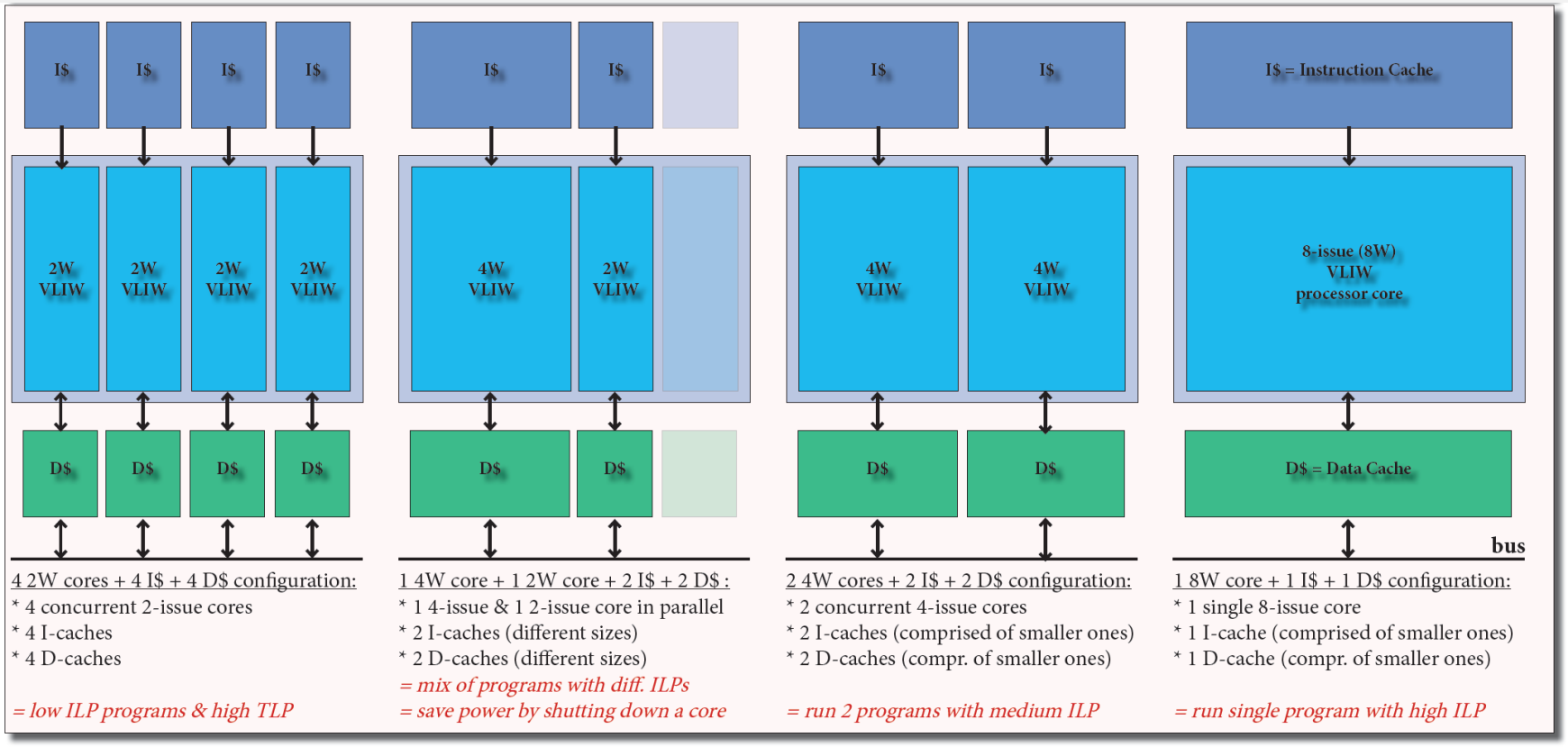
The Liquid Processor (ρ-VEX)



Current status:

- Many MSc students involved
- New fault-tolerance techniques implemented
- MMU finalized
- Multiple compilers (LLVM, GCC, Open64, Cosy, HP)
- 2 simulators

- Linux-based system controlling several ρ-VEX cores (multi-/many-core)
- ASIC design
- Gaming
- RTOS

Potential ρ-VEX MSc project topics

MSc projects:

- Develop **new scheduling mechanisms** (in OS or hardware)
- Develop **new compiler techniques** for a dynamically changing processor
- Implement communication mechanisms for **compiler information → HW & OS**
- Implement **security techniques** against side-channel attacks
- **Build a "generic RISC processor"** on top of our dynamic VLIW microarchitecture
- Implement **fine-grain reconfiguration** to extend processor capabilities
- Introduce **MOLEN instructions** into the ρ-VEX processor
- Perform measurements of the **Application-Specific Integrated Circuits (ASIC)**-port with regards to power, energy, and performance

Take part in the development of a new and exciting processor design!!

More concrete MSc project examples

MSc project 1: **Distributed Reconfigurable & Parameterized Computing**
- Connect multiple ρ-VEXes over the Internet to collaboratively perform computing
- Implement a simple OS to allow for communication between distributed ρ-VEXes

MSc project 2: **Secure ρ-VEX Processor against Side-channel Attacks**
- Utilize the reconfiguration capabilities to prevent side-channel attacks

MSc project 3: **Hardware Binary Translation Unit**
- Implement a binary translation unit in hardware (targeting MIPS, ARM, RISC-V ISAs)

MSc project 4: **Design the fastest ρ-VEX Processor**
- (Re-)Design the existing core purely for speed

MSc project 5: **Code Optimizations to increase ILP**
- Investigate compiler algorithms/heuristics that lead to improved ILP

MSc project 6: **Develop Models of ρ-VEX for Mainstream Simulators**
- Generate models of the ρ-VEX processor for the gem5 simulation platform

Reconfigurable In-Memory Computing

Potential MSc projects:

- Implement digital periphery to extend memristor array functionalities
- Build a digital controller on FPGA connected to a memristor array
- Extend compute-in-memory simulator to target different memristor technologies

Collaboration Erasmus MC (Rotterdam, NL)

Topic 1: Implantable Medical Devices (IMDs)

- Work on (co-)processors, compilers, SoC design

Topic 2: HPC Brain Simulations *(initial ideas)*

- Porting of brain models onto Maxeler DFEs, GPUs, Xeon-Phi's
- Performance and power characterization of brain-related workloads towards developing cost prediction models for use in datacenter/HPC facilities
- Multiple Fixed-Point analysis of compute-intensive brain-modeling kernels for execution on (multiple) FPGAs
- Coarse-grain reconfigurable substrates suitable for brain-model kernels towards higher performance, lower power and shorter (partial) reconfiguration times.

Other topics in different medical fields are available – check Brightspace page!

Building a RISC-V infrastructure

Potential MSc projects:

- Evaluate different open-source RISC-V cores to build an embedded SoC
- Build a compiler infrastructure
- Build a parameterized core (suitable for future labs)
- Evaluate different simulators (including GEMS) and integrate with our existing compute-in-memory simulator